UGPHS-05

BLOCK-1

Network Analysis And Devices

Utter Pradesh
Rajarshi Tandon Open University

UGPHS-05
Electrical Circuits and Electronics

Block

1

NETWORK ANALYSIS AND DEVICES

COURSE INTRODUCTION

Electronics plays a major role in almost every sphere of our life-our homes, factories, offices, banks, shops and hospitals. It is being used more and more in entertainment, communication, defence, industrial sector, medical sciences, instrumentation etc. Its importance increases with every advance in technology and with the urge to computerise human tasks and industrial processes. Electronics is a fast changing area and a thorough grounding in the subject fundamentals is absolutely necessary.

"Electrical Circuit and Electronics" is a 4-credit elective course in the Physics discipline for students of Bachelor's Degree Programme. This course is intended for any student who has had a physics course at 10+2 level. The whole course covers broadly the following four areas:

1. **Network Analysis and Devices**

   In this topic there are three units: Unit 1-Circuit analysis:
   Unit-2: DC and AC circuit; Unit 3-Electron devices.

2. **Electronic Circuits**

   It has three units viz. Unit 4-Amplifiers; Unit 5-Oscillators;
   Unit 6-Power supply.

3. **Linear Integrated Circuits**

   There are three units viz. Unit 7-The operational amplifier; Unit 8-Application of operational amplifier and Unit 9-Linear IC-amplifier and Voltage regulator.

4. **Digital Electronics**

   This topic is covered in four units viz. Unit 10-Number system and codes; Unit 11-Fundamentals of Boolean Algebra and Flip Flops; Unit 12-Counter, Register, memory circuit and Analog/Digital circuit and Unit-13 Electronic Instruments.

   One last word about how to study the course material.

Study Guide

The best way to learn a subject is to solve problems. We have given many solved examples, self-assessment questions and terminal questions. Answer to SAQ's and TQ's are given at the end of each unit.

After reading a section of a particular unit ask yourself-What have I learnt. Attempt all self-assessment questions. Don't skip any of them as they are designed to assess your understanding of the subject. But don't get tempted to look at the answers given at the end of each unit before you try out the SAQ's and terminal questions!

Some of the abbreviations used in the text are Fig. for Figure, Sec. for Section, Eq. for Equation, SAQ for self-assessment questions and TQ for terminal questions. For example, Fig. 1.5 refers to fifth figure in unit 1. Similarly, Sec. 2.7 is seventh section in unit-2 and Eq. 3.4 in the fourth equation in unit-3.

This is a 4-credit course which means that you have to put in 120 hours of work. Of these, you should spend about 80 hours to study course material and solve SAQ's and TQ's. The remaining time is intended for assessment and counselling sessions. We hope that you will enjoy the subject. We wish you success.

Some reference books, which you may find useful, are given below:

1. Electronic Principles - A.P. Malvino
2. Electronic for Sciences - T.R. Vishwanathan, G.K. Mehta and V. Rajaraman
3. Introductory Electronics for Scientists and Engineers - R.K. Simpson
4. Digital Principles and Applications - A.P. Malvino, and D.P. Leach

BLOCK 1 NETWORK ANALYSIS AND DEVICES

In your School syllabus you have studied the various laws to deal with simple electric circuits like Ohm's law and Kirchoff's laws. Sametimes the circuits are so complicated that these can't be simplified using these laws or the calculations are very lengthy which can be done at the cost of a lot of time. The Radio, Television, Computer etc. contain very complicated circuits. To determine the current in any element is very complicated using above laws. In Unit 1 we will discuss some special kind of networks and theorems which are very useful in reducing the complicated circuits to simple form and then direct calculate the current in any circuit element.

In Unit 2, you will study RLC resonant circuits, fitters, and attenuators.

In Unit 3 you will study various electronic devices. Some of these are already familliar to you in the lower classes. These devices are the basic pillars of the foundation of electronics. Thus we will first recapitulate them before proceeding to the higher devices like transistors, FET, MOSFET etc. and their applications.

UNIT 1 CIRCUIT ANALYSIS

Structure

1.1 INTRODUCTION

Developments in the field of electronics can be considered to be one of the great success stories of this century. Beginning with crude spark-gap transmitters and "cat's-whisker" detectors at the turn of the century we have passed through a vacuum tube era of considerable sophistication to a solid-state era in which flood of stunning advances shows no signs of abating.

In order to understand the marvels of electronics, we must start with the study of the laws, rules of the thumb and tricks that constitute the art of electronics as we see it. It is necessary to begin with talk of voltage, current, power and component that make up electronic circuits. To visualise, in a simple manner, an electric circuit consists of three parts: (i) Energy Source such as battery or generator (ii) the load or sink such as lamp or motor and (iii) connecting wires. The purpose of this circuit is to transfer energy from source to the load. Using this example, we can define an electric network as basically interconnection of two or more simple circuit elements viz voltage source, resistors, inductors or capacitors. If the network contains at least one closed path, it is called an electric circuit. In this unit, we shall be studying the basic laws which govern the transfer of energy from source to load, some important theorems and simplifications at which we arrive after going through these laws, in order to understand functioning of a given electric circuit, which forms basis of any modern electronic gadget.

Objectives

After studying this unit, you should be able to

- explain the concepts of voltage and current sources,
- apply Kirchoff's law, Thevenin and Norton theorem to simplify given network,
- state and apply Superposition, reciprocity and Maximum power transfer theorem to a given network.

1.2 CIRCUIT ELEMENTS

A network is a connection of elements to obtain a certain performance. In circuit analysis, we are interested in electrical networks in which passive elements such as resistors, inductors and capacitors are appropriately connected to voltage and current sources. These elements and sources are idealizations to actual elements and sources. The idealization enables an effective analysis of the network. The problem in network analysis is to analyse the given network and to determine the voltages and currents through various elements. Broadly, network elements may be classified into four groups:

(i) Active or passive

(ii) Unilateral or bilateral

(iii) Linear or nonlinear

(iv) Lumped or distributed

Active or passive: Energy sources (voltage or current sources) are active elements, capable of delivering power to some external device. Besides energy sources there are many other components used in electronic circuits which fall under the category of active elements. These components can be classified into two: tubes (both vacuum tubes and gas tubes) and semiconductor devices which include junction diode, transistor, field effect transistor, UJT, SCR, zener diode etc.

The passive elements are those which are capable only of receiving power like resistors, inductors, or capacitors. Some passive elements like inductors and capacitors are capable of storing a finite amount of energy, and return it later to an external element.

Bilateral or unilateral: We know that electrical characteristics of passive elements are best described by current-voltage relationship. In the bilateral elements, the voltage - current relation is the same for current flowing in either direction e.g. resistors. In contrast, a unilateral element has diffferent relation between voltage and current for the two possible direction of current e.g., diodes.

Linear or non-linear: An element is said to be linear, if it satisfies the linear voltage — current relationship implying that if the current through the element is scaled up by a factor, the voltage across the element also gets scaled up by the same factor. For example, the $V - I$ relation for resistor is $V = IR$ and is linear. All elements which does not satisfy this relation is called nonlinear elements such as Diode. The $V - I$ relation for diode is given by

$$I = I_o [e^{qv/kt} - 1]$$

which is clearly non-linear.

Lumped or distrlbubuted : The elements which are separated physically are known as Lumped elements like resistors, capacitors or inductors. Distributed elements on the other hand are those which are not separable for analytical purposes for example a transmission line which has distributed resistance, inductance and capacitance along its length.

V–I relations:

(a) **Resistor** : See Fig 1.1.

(i) $V = IR \rightarrow I = GV$

where $G = I/R$ = conductance and V & I are time independant voltage and current.

(ii) $V(t) = i(t) R$

where $V(t)$ and $i(t)$ are time dépendent voltage and current.

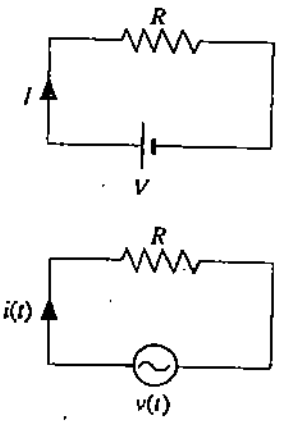


Fig. 1.1: *V–I* relationship for resistor.

(b) **Inductor** : See Fig 1.2.

For inductor, the flux is given by

$$\phi \alpha i$$

$$\rightarrow \phi = Li$$

where L is coefficient of self inductance. Differentiating above expression with time, we get

$$\frac{d\phi}{dt} = L\frac{di}{dt}$$

As per Lenz's law, rate of change of flux is potential,

$$\therefore \quad V = L\frac{di}{dt}$$

(i) For time independent voltage and current,

$$\frac{di}{dt} = 0$$

$$\therefore \; V(t) = 0$$

which implies that for DC voltages and currents, under steady state (after long lapse of time) conditions, the voltage across inductor will be zero implying, it will behave as a short circuit.

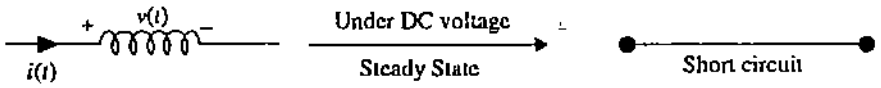


Fig. 1.2: *V-I* relationship for Inductor.

(ii) For time dependent voltage and current, the relationship is given by

$$V(t) = L\frac{di(t)}{dt}$$

(c) **Capacitors** : See Fig 1.3. For a capacitor $Q \alpha V$

$$\rightarrow Q = CV$$

where C is called capacity of capacitor. Differentiating with respect to time, we get

$$i = \frac{dQ}{dt} = C\frac{dV}{dt}$$

(i) For time independent current & voltage (i.e., for dc)

$$\frac{dV}{dt} = 0$$

This suggests that for time independent current and voltage, the capacitor under steady state (after long lapse of time) will behave as open circuit because $i = 0$.

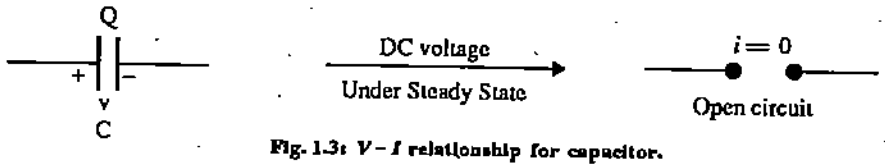


Fig. 1.3: $V - I$ relationship for capacitor.

(ii) For time dependent current and voltages the current - voltage relationship is given by

$$i(t) = C\frac{dV(t)}{dt}$$

(d) **Energy sources:**

There are two categories of energy sources.

(i) Independent Energy Source

(ii) Dependent Energy Source

(f) Independent Energy Source:

As you know independent energy source can be of two types: Voltage sources and current sources. Independent voltage or current sources are one for which voltage and current are fixed and are not affected by other parts of the circuit.

An ideal voltage source is a two terminal element in which the voltage V_a is completely independent of the current i_a through its terminals. The representation of ideal voltage source is shown in Fig. 1.4.

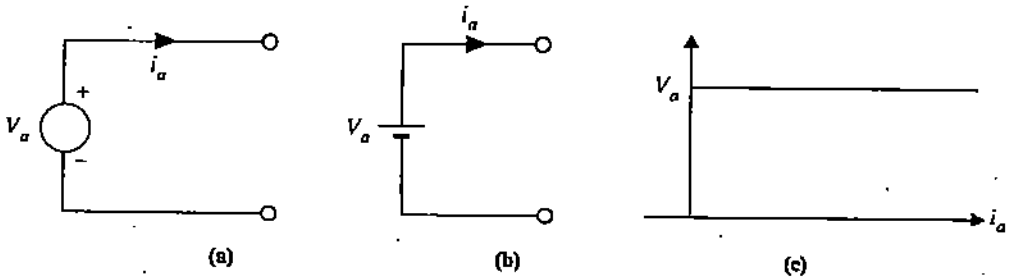


Fig. 1.4: Ideal voltage source.

If we observe $V - I$ characteristics for an ideal voltage source as shown in Fig. 1.4(c), at any time, the value of the terminal voltage V_a is constant with respect to the current value i_a. But for a practical voltage source, its internal resistance is in series with the source as shown in Fig. 1.5 and its terminal voltage falls as the current through it increases. The terminal voltage depends on the source current because, $V_{terminal} = V_S - i_s R$.

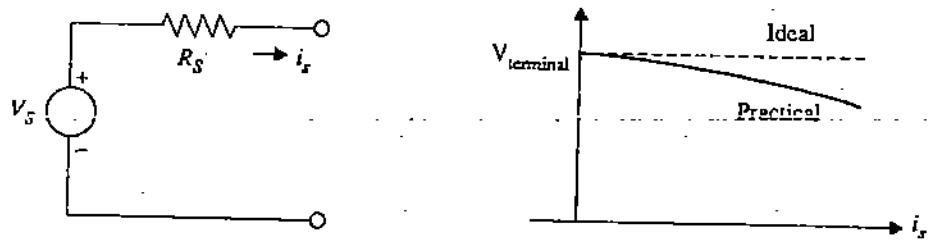


Fig. 1.5: Practical voltage source.

An ideal independent current source is a two terminal element in which the current is completely independent of the voltage V_s across its terminals. The representative of ideal current source is shown in Fig. 1.6.

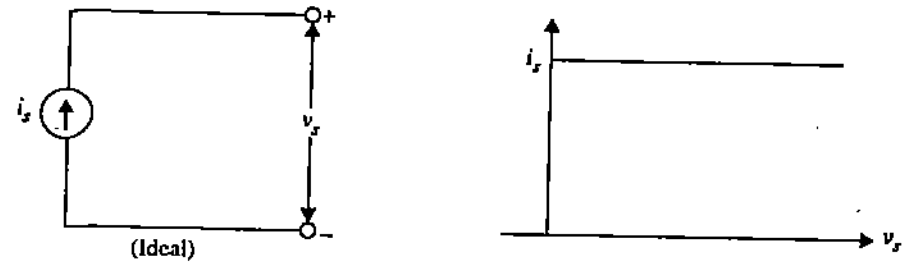


Fig. 1.6: Ideal current source.

In practical current sources, the internal resistance is shown in parallel with the source as shown in Fig.1.7. In this case, the magnitude of current falls, as the voltage across its terminals increases. The terminal current is given by

$$I_{terminal} = i_S - \left(\frac{V_S}{R}\right)$$

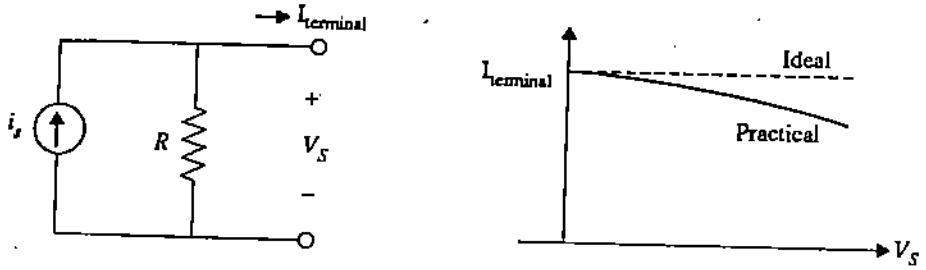


Fig. 1.7: Practical current source.

Dependent Sources

In case of dependent sources (voltage or current), the source voltage or current is not fixed but is dependent on the voltage or current existing at some other location in the circuit. These sources mainly occur in the analysis of equivalent circuits of active devices such as transistors. The symbols for dependent circuit voltage and current sources are shown in Fig. 1.8.

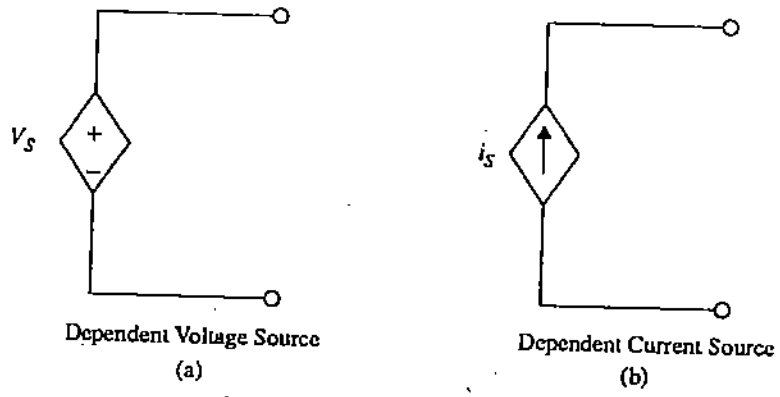


Fig. 1.8: (a) Dependent voltage source (b) dependent current source.

1.3 KIRCHOFF'S LAWS

There are two fundamental laws which are satisfied by electrical networks. These are Kirchoff's Current Law (KCL) and Kirchoff's Voltage Law (KVL). These form the basis of circuit analysis. You have already studied these laws at the school level. However, we will recapitulate them as they are very important for circuit analysis.

Kirchoff's Current Law (KCL)

It states that the algebraic sum of currents at a node (or junction) is equal to zero. Alternate form of KCL are:

Algebraic sum of currents entering a node = 0

Algebraic sum of currents leaving a node = 0

or sum of currents entering a node = sum of currents leaving a node

In order to apply KCL, we have to make a convention for currents because we have to take algebraic sum.

Convention : All entering currents are treated positive (+) and leaving currents as negative (–).

Example 1

In Fig. 1.9. write KCL for the various nodes (currents are marked).

Solution

Clearly 1, 2, 3, 4, 5 represents nodes, we shall now write KCL for all the nodes.

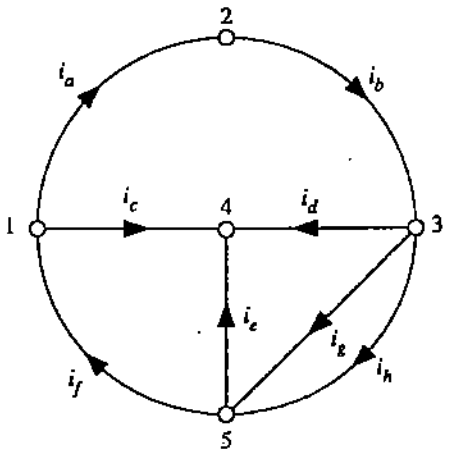


Fig. 1.9:

At node 1, $-i_a - i_c + i_f = 0$ [using conventions stated earlier]

At node 2, $i_a - i_b = 0$

At node 3, $-i_b - i_d - i_g - i_h = 0$

At node 4, $i_c + i_d + i_e = 0$

At node 5, $i_h + i_g - i_e - i_f = 0$

It is very interesting to note that the KCL at node 5 can be obtained simply by summing the KCL equations for all the other nodes (1 to 4). We observe the following from this exercise:

(i) It is enough to write KCL for all nodes but one.

(ii) The KCL for the excluded node is not independent as it can be obatined from the KCL written for the other nodes.

Remember : It is sufficient to write KCL for $(n - 1)$ nodes for a network having n nodes.

Kirchoff's Voltage Law (KVL)

It states that the algebraic (with proper sign) sum of voltages in a closed network is zero. In order to apply this law, we must know the magnitude and polarity of all the voltages in that closed network. In order to make our life simple, we follow a convention that for any passive element (R, L or C), if current is entering at a terminal, it will have +ve potential and the terminal where current is leaving is

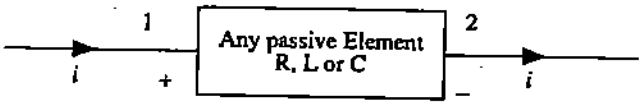


Fig .1.10. : Convention for KVL.

regarded as –ve potential. (See Fig. 1.10)

As an example we apply KVL in a network shown in Fig. 1.11 with marked voltage polarity given along with their values :

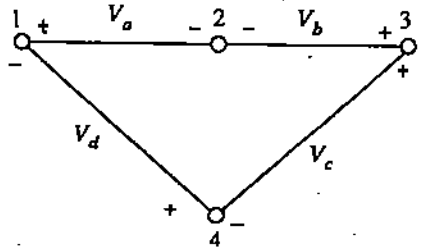


Fig. 1.11:

Applying KVL, we get,

$$V_a + (+V_d) + (V_c) + (-V_b) = 0$$

We have used V_a as reference voltage.

Remember :

1. Once you have chosen reference potential always come out from +ve terminal of that potential to move into other parts of network. Sometimes it may be clockwise or anticlockwise. You need not worry about it.

2. In order to determine the proper sign of voltages, you follow the following :

   While coming out from +ve terminal of ref. pot, if you encounter first the +ve terminal of next element, treat it as –ve. But if you encouter –ve terminal of the next element, treat it as +ve.

Simplifications based on KCL, KVL

In circuit analysis, the commonly used simplifications based on KCL and KVL are as follows:

1. The same current flows in elements connected in series.

2. The same voltage exists across elements connected in parallel.

3. A resistor R connected across a voltage source V_s has a voltage V_s and hence the current in that resistor element is V_s/R.

4. An element in series with a current source I_s has a current I_s flowing through it, so that the voltage across such a resistor element is $V = I_s R$.

Example 2

In the circuits shown in Fig. 1.12, obtain the indicated variable. Use simplifications listed above.

Solution:

(a) R_1 and R_2 are in series and hence, have the same current I. Apply KVL,

$$V_s - R_1 I - R_2 I = 0$$

$$\rightarrow \quad V_s = (R_1 + R_2) I \qquad (1)$$

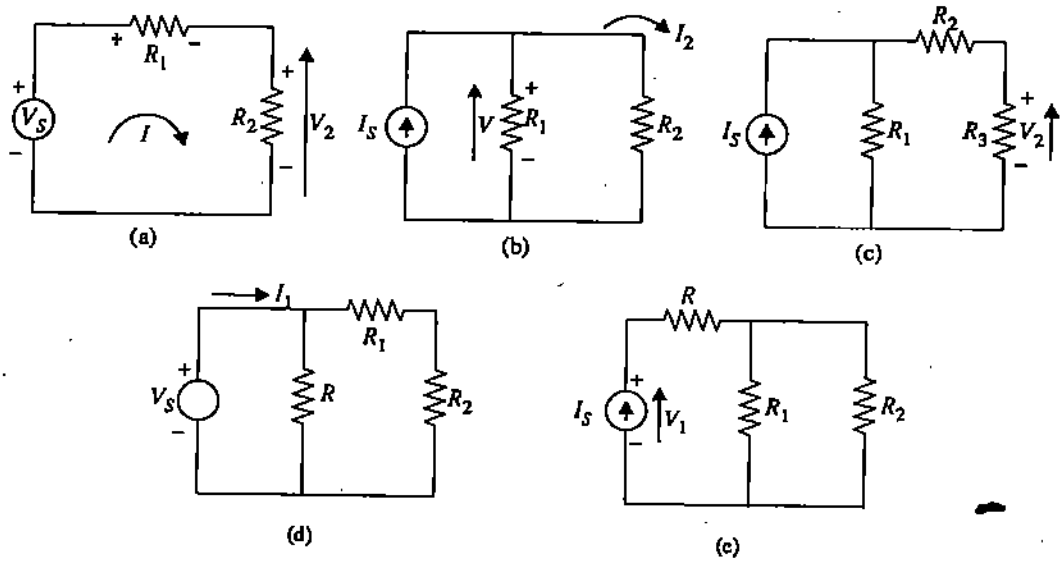


Fig. 1.12:

Also, $V_2 = R_2 I$ (2)

Solving (1) and (2), we get

$$V_2 = V_s \frac{(R_2)}{(R_1+R_2)}$$

This is **'voltage divider'** action.

(b) Since R_1 and R_2 are in parallel, they have same voltage V across them. Apply KCL,

$$I_s = \frac{V}{R_1} + \frac{V}{R_2} \quad (3)$$

Also, $I_2 = \frac{V}{R_2}$ (4)

solving (3) and (4), we get

$$I_2 = I_s \frac{R_1}{(R_1 + R_2)}$$

This result is known as **"current divider"** action.

(c) Notice that R_2 and R_3 are in series so that $(R_2 + R_3)$ is in parallel with R_1. Hence, the current in $(R_2 + R_3)$ can be found out using current divider principle and is given by

$$I = I_s \frac{R_1}{(R_1 + R_2 + R_3)}$$

Also, $V_2 = R_3 I$

$$= I_s \frac{R_1 R_3}{(R_1 + R_2 + R_3)}$$

(d) The circuit is the same as in (a) except for the resistor R across V_s. R draws a current $\frac{V_s}{R}$, Hence the current drawn from V_s is now :

$$I_1 = \frac{V_s}{R} + \frac{V_s}{(R_1 + R_2)}$$

(e) The circuit is same as in (b) except for the resistor R in series with I_s. Also R_1 and R_2 are in parallel.

$$\therefore \quad V_1 = I_s R + I_s \frac{R_1 R_2}{R_1 + R_2}$$

SAQ 1

Determine V for the circuit shown in Fig. 1.13.

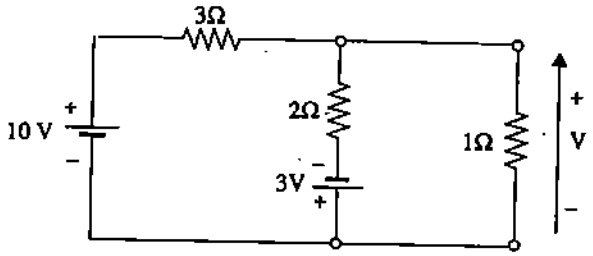


Fig. 1.13:

SAQ 2

In the circuit shown in Fig. 1.14, determine R so that $i = 1$

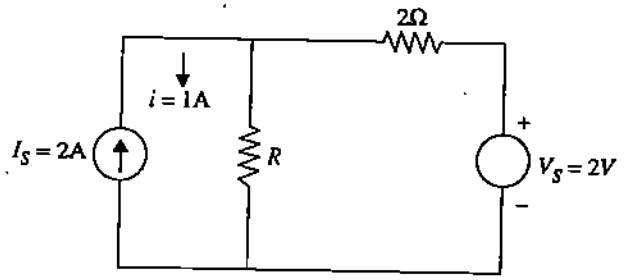


Fig. 1.14:

1.4 COMPLEX IMPEDANCES

So far the discussions have been confined to resistive circuits. Resistance restricts the flow of current by opposing free electron movement. Each element has some resistance, for example, inductance has some resistance and capacitance also has some resistance. In resistive element, there is no phase difference between voltage and current whereas in inductive circuit, voltage leads over current and in capacitative circuit, current leads over voltage. The comlex impedance of a network is given by

$$Z = R + j X$$

where Z = Complex Impedance

R = Resistance

X = Reactance

$$|Z| = \sqrt{ZZ^*} = \sqrt{R^2 + X^2}$$

and $$\angle Z = \frac{X}{R} = \frac{\text{Imaginary part}}{\text{Real part}}$$ (as shown in Fig. 1.15)

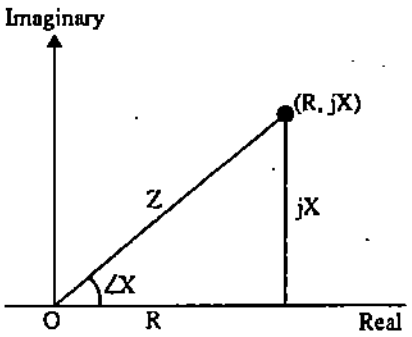


Fig. 1.15:

Example 3: In *RL* network as shown in Fig. 1.16

$$Z = R + j\omega L$$

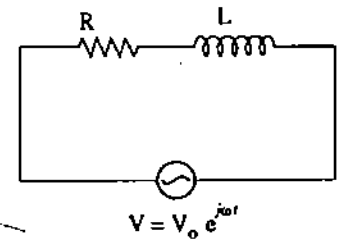


Fig. 1.16: *RL*-network

$$|Z| = \sqrt{R^2 + \omega^2 L^2}$$

$$\angle Z = \frac{\omega L}{R}$$

Example 4: In *RC* network as shown in Fig. 1.17

$$Z = R + \frac{1}{j\omega C} = R - \frac{j}{\omega C}$$

$$|Z| = \sqrt{R^2 + \frac{1}{\omega^2 C^2}} \quad \text{and} \quad \angle Z = -\frac{1}{\omega C R}$$

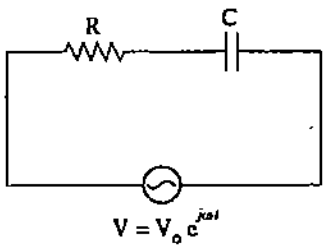
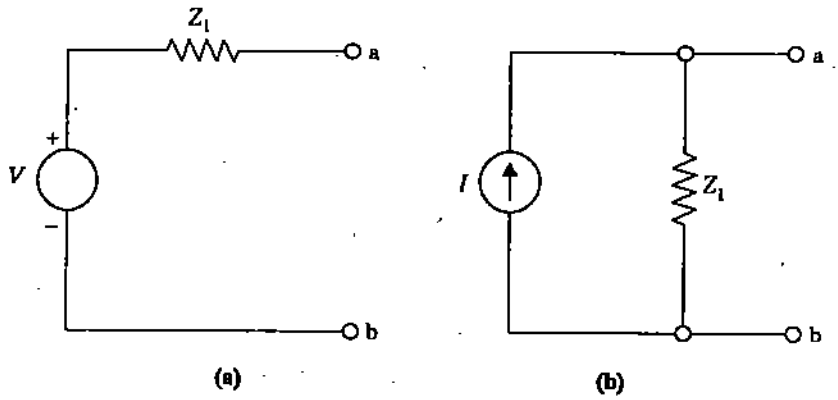


Fig. 1.17: *RC* network.

1.5 CURRENT-VOLTAGE SOURCE TRANSFORMATIONS

We have studied earlier that an independent energy source is either of voltage type or of current type. Moreover, a practical source is non-ideal in nature. We can represent a practical voltage source by an ideal voltage source having a series impedance (generally, a resistance), as shown in Fig. 1.18a. Also we can approximate a practical current source by an ideal current source with a shunt impedance [Fig. 1.18b].

These representations account for the fall in terminal voltage with an increase in output current (due to decrease of load impedance) for the voltage source, and for a fall in the output current with an increase of load resistance for the current source.



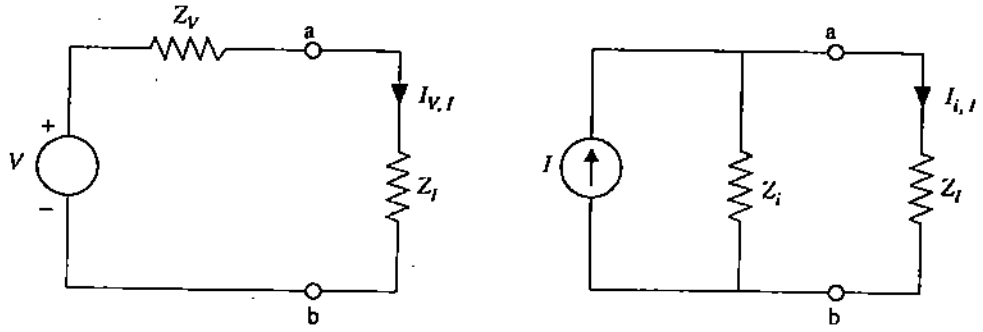
(a) (b)

Fig. 1.18: A practical form of (a) voltage source (b) current source.

In many network analysis problems, it is found that the conversion, of voltage source into an equivalent current source or vice versa, i.e., source transformation, makes the problems considerably simpler. In this section, we shall derive the conditions for the equivalence of practical voltage and current sources.

Let us consider Fig. 1.19a, where a voltage source is shown connected to a load Z_1. The current, delivered to the load, is given by

$$I_{v,1} = \frac{V}{Z_V + Z_1} \tag{1.1}$$



(a) (b)

Fig. 1.19: (a) Voltage and (b) current source with load Z_1.

Now, if we connect the same load Z_1 across the current source as shown in Fig. 1.19b then the current delivered to the load is given by

$$I_{i,1} = \frac{Z_i}{Z_i + Z_1} I \tag{1.2}$$

In case the two energy sources are equal, then the respective current, delivered to Z_1 must be equal, i.e., $I_{v,1} = I_{i,1}$. From Eqs. (1.1) and (1.2), we have

$$\frac{V}{Z_V + Z_1} \quad \frac{Z_i I}{Z_i + Z_1} \tag{1.3}$$

Eq. (1.3) will be satisfied, if

$$I = \frac{V}{Z_i} \quad \text{and} \quad Z_V = Z_i \tag{1.4}$$

Statement of the Conversion Principle

A constant voltage source of voltage V and series impedance Z_V is equivalent to the constant current source of current, $I = V/Z_V$ and shunt impedance Z_V.

1.6 SUPERPOSITION THEOREM

The basic priciple of superposition states that if the effect produced in a system is directly proportional to the cause, then the overall effect, produced in the system due to the number of causes acting jointly, can be determined by superimposing (adding) the effects of each source acting separately. It is important for us to note that the above principle form the foundation of many engineering systems, such as the broadcasting system, audio system etc. For example, in a large orchestra, we would like the net response of the system to be the sum of individual responses of each instrument played separately. In other words, good fidelity of the system depends upon the validity of the superposition principle.

As the superposition principle is only applicable on linear networks and systems, it is important for us to first clearly understand the term 'linear' before proceeding with the formal presentation and proof of the superposition theorem.

We can call a device linear, if it is characterized by an equation of the form :

$$y = mx \tag{1.5}$$

Where m is a constant. For example, a wire-wound inductor is linear device ; and its variables are V and i. Eq. (1.5) also implies that y is proportional to x, (You should clearly note that the general superposition principle stated earlier is dependent of proportionality). A Network / system, which contains only linear devices (or elements), is called a linear network / system.

1.6.1 Statement of Superposition Theorem

In a linear network, having several sources (which include the equivalent source due to initial conditions), the overall response, at any point in the network, is equal to the sum of individual responses of each source considered separately, the other sources being made inoperative.

Remarks

(1) We observe that the theorem basically implies that the total response in a linear circuit is a proper summation of the partial responses of the sources, considered one at a time.

(2) By the term source, we include all the voltage and current sources and also the equivalent source constituted by the initial conditions in the network.

(3) We make the source inoperative by (a) short-circuiting the voltage sources and replacing them by their series impedances and by (b) open-circuiting the current sources and substituting them by their shunt impedances.

(4) The linear network comprises of independent sources, linear dependent sources and linear passive elements like resistors, inductors, capacitors and transformers. Moreover, the components may either be time-varying or time-invariant.

(5) We find that the main advantage of superposition theorem lies in the fact that it allows solution of networks without the need of setting up large number of circuit equations. This is possible as only one source is considered at a time.

(6) The superposition theorem seems to be so apparent that one tends to apply it at places where it is not applicable.

1.6.2 Proof of Superposition Theorem

Let us consider a linear network N having L independent loops. The loop equations are :

$$
\begin{aligned}
Z_{11} I_1 + Z_{12} I_2 + \cdots + Z_{1L} I_L &= E_1 \\
Z_{21} I_1 + Z_{22} I_2 + \cdots + Z_{2L} I_L &= E_2 \\
\cdots \quad \cdots \quad \cdots \quad \cdots \quad \cdots & \\
Z_{L1} I_1 + Z_{L2} I_2 + \cdots + Z_{LL} I_L &= E_L
\end{aligned}
\qquad (1.6)
$$

The solution of Eq. (1.6) is of the following form :

$$
\begin{aligned}
I_1 &= Y_{11} E_1 + Y_{12} E_2 + \cdots + Y_{1L} E_L \\
I_2 &= Y_{21} E_1 + Y_{22} E_2 + \cdots + Y_{2L} E_L \\
\cdots \quad \cdots \quad \cdots \quad \cdots \quad \cdots & \\
I_L &= Y_{L1} E_1 + Y_{L2} E_2 + \cdots + Y_{LL} E_L
\end{aligned}
\qquad (1.7)
$$

Now we apply the superpostion theorem.

First we assume all E's, except E_1, to be zero. This will give current in loop 1 as $Y_{11} E_1$, in loop 2 as $Y_{21} E_1$, etc. Similarly, when all the sources except E_2 are made inoperative, the current in loop 1 is $Y_{12} E_2$, loop 2 is $Y_{22} E_2$, and so on. The procedure is repeated in turn for the remaining sources E_3, E_4, etc. On applying the superposition principle, the individual responses are added together to give the resulting responses. For example, we have for the first loop

$$I_1 = Y_{11} E_1 + Y_{12} E_2 + \cdots + Y_{1L} E_L$$

But this result is the same as that obtained by solving the simultaneous Eq. 1.7. A Similar proof, can be given based on junction method.

SAQ 3

Using the superposition theorem, find the current (I) in the branch AB of Fig. 1.20.

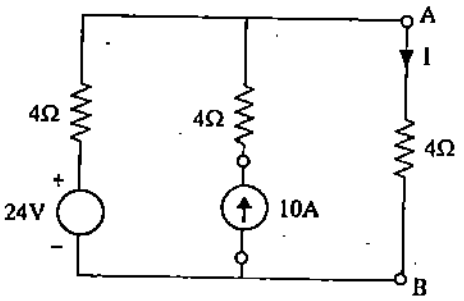


Fig. 1.20:

1.7 RECIPROCITY THEOREM

The reciprocity phenomenon is commonly found in nature. Besides in electrical circuit we also observe this phenomenon in mechanics, acoustics, etc. When it is applicable to a physical system, we can interchange the excitation and the response points without changing the response, of the system, to a given excitation. It finds wide utility in the analysis and design of systems and also in the area of measurements. For a better understanding, let us consider the example of a telephone line between two subscribers X and Y. If the telephone circuit comprises permissible elements, then the reciprocity theorem permits us to assume that the transmission from X to Y is identical to that from Y to X. This greatly simplifies, in practice, the design and testing of the line.

1.7.1 Statement of Reciprocity Theorem

Reciprocity theorem states that if we consider two loops A and B of a reciprocal network N, and if an ideal voltage source, E, in loop A, produces a current I in loop B, then an identical source in loop B will produce the same current I in loop A.

The dual is also true. If we consider two node pairs AA′ and BB′ of a reciprocal network N and an ideal current source of I amp applied to the node – pair AA′ produces a voltage V at the node – pair BB′ then an identical current source at BB′ will produce the same voltage V at AA′.

Remarks

(1) A reciprocal network comprises of linear time-invariant, bilateral, passive elements. It is applicable to resistors, capacitors, inductors (including coupled inductors) and transformers. However, both dependent and independent sources are not permissible. Also, we are considering only the zero-state response by taking the initial conditions to be zero. In this sense, the theorem is more restrictive than the superposition theorem.

(2) The superposition theorem seems to be more obvious to most people and, hence, is easily acceptable. As pointed out earlier, we have to be more careful not to apply it at the wrong place. On the other hand, the reciprocity theorem is far less obvious.

1.7.2 Proof of Reciprocity Theorem

Let us consider a network N having only one energy source driving a voltage E_1. We can number the loop in which the source is present as 1 and that in which the response is to be determined as 2. The second Equation from Eq. (1.7) gives

$$I_2 = Y_{21} E_1 \tag{1.8}$$

Next we reduce E_1 to zero and place a voltage source E_2 in loop 2. Now, the first of Eq. (1.7) gives

$$I_1 = Y_{12} E_2 \tag{1.9}$$

In case the two sources are identical, i.e., $E_1 = E_2$, then I_1 will also be equal to I_2 provided that $Y_{12} = Y_{21}$. As $Y_{21} = Y_{12}$, in all linear, bilateral networks, we have proved the reciprocity theorem.

SAQ 4

In the circuit of Fig. 1.21, determine the current in the 4-ohm resistor. Verify the reciprocity therorem.

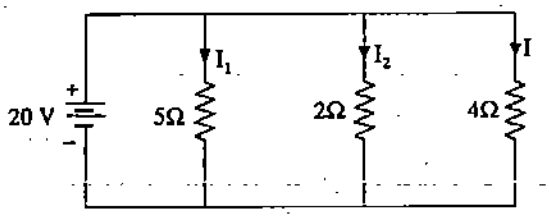


Fig. 1.21

Also, find the change in current in the 5-ohm resistor, when the points of excitation and response are interchanged.

1.8 THEVENIN'S THEOREM

Thevenin's theorem is one of the most important theorems in Circuit Theory. It provides us with a powerful technique of calculating the response in a complicated network, particularly when one part of the network (generally called the load) is varying, while the remaining parts remain fixed. In addition, it also helps us in getting a better insight of any linear network as seen from the terminals across which the load is connected.

1.8.1 Statement of Thevenin's Theorem

A two-terminal linear active network may be replaced by a voltage source in series with an impedance. The emf of the voltage source (V) is the open-circuit voltage at the terminals and the impedance (Z) is that viewed at the terminals when all the generators, in the network, have been replaced by their internal impedances.

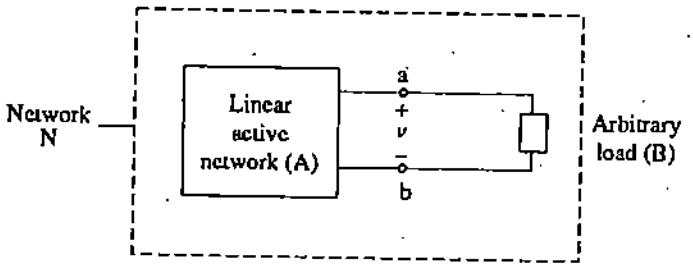


Fig. 1.22: Original network.

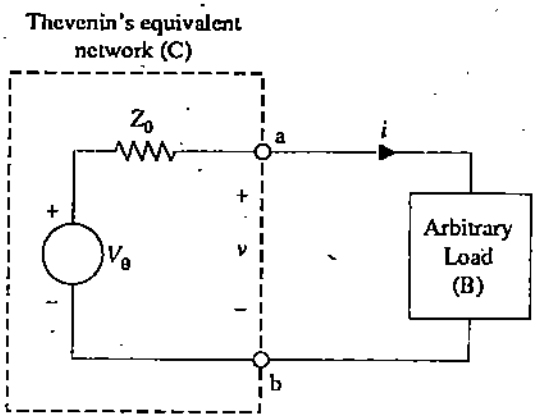


Fig. 1.23: Thevenin equivalent of Fig. 1.22.

Explanations and Remarks

Let us consider the network N shown in Fig. 1.22. It consists of two parts : a linear active network A and an arbitrary network B, called the load. We assume that the only interaction, between the two networks, is through the load current (I), i.e., no magnetic coupling or coupling through dependent source is present between A and B. According to the Thevenin's theorem, we can replace the active network A by the Thevenin's equivalent generator and a series impedance. The voltage of this generator (V_θ) is the open-circuit voltage across, a-b, when the load is disconnected. It is caused by the energy sources, in A, including the initial conditions. (This voltage is the one which a VTVM records across a-b). The equivalent series impendance (Z_θ) is the impedance across a-b when all the independent sources are reduced to zero by replacing the voltage sources by short-circuits, open-circuiting the current sources and setting the initial conditions to zero. The dependent sources are left unaltered. (In fact, an impedance bridge across a-b will measure this impedance Z_θ). The Thevenin's equivalent of Fig. 1.22. is shown in Fig. 1.23. In case the load B simply consists of an effective impendace Z_l, the load current is given by -

$$I_l = \frac{V_\theta}{Z_\theta + Z_l} \tag{1.10}$$

we should take note of the following points.

(i) We only require network A to be linear : it may include time-varying elements.

(ii) We place no restriction on the load except that :

(a) it had no coupling with A except for the load current and

(b) the complete network had a unique solution.

1.8.2 Proof of Thevenin's Theorem

Let us consider the circuit of Fig. 1.24, where the active network A (having an open-circuit voltage V_0 is driving a current into a passive load B. We assume the load current as I, the effective impedance, offered by the load as, Z_O.

Next, a voltage source E_1 is introduced in series with the load, as shown in Fig. 1.24. It is adjusted such that the current I becomes zero. Under such a

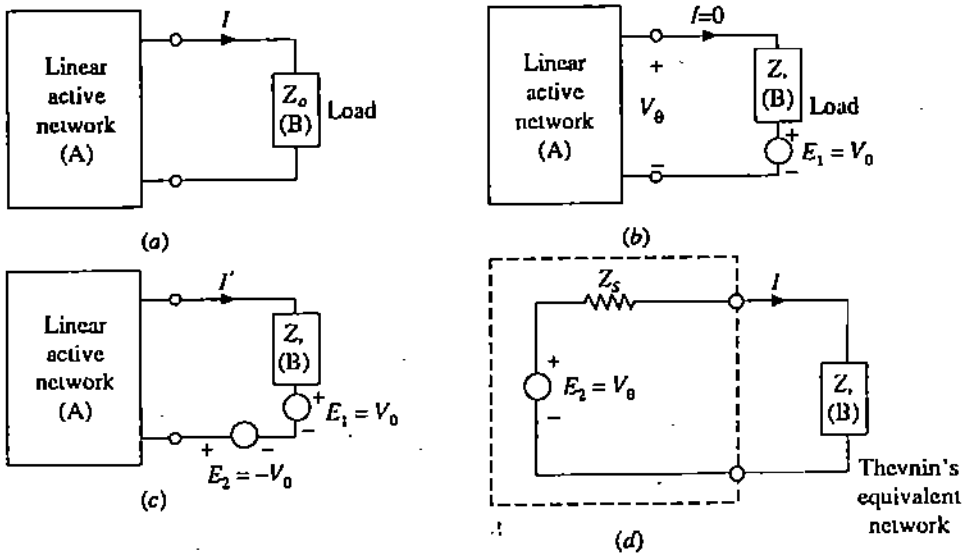


Fig. 1.24: Circuits required in the proof of Thevenin's theorem.

condition, the network is practically under-open circuit condition : and the balancing voltage required is $E_1 = V_\theta$.

Now we place another voltage source E_2 in opposition to E_1 but equal in magnitude, i.e., $E_2 = -V_\theta$. This results in a current I'. Since the net voltage across E_1 plus E_2, is zero, the circuits of Fig. 1.24a and 1.24c are equivalent : and $I' = I$. This also implies that the current, due to E_2 alone (after making the sources in A inoperative and replacing it by its impedance Z_θ), is given by

$$I = \frac{E_1}{Z_\theta + Z_o} = \frac{V_\theta}{Z_\theta + Z_o} \tag{1.11}$$

The process is depicted in Fig. 1.24d, where the network A has been replaced by a voltage generator of voltage V_o and a series impedance Z_o. This proves Thevenin's theorem for passive load.

In case the load is active, Thevenin's theorem is still valid. The proof is based on the lines of passive load, with the difference that now we have to apply voltage source E_1 so as to balance the combined effects of V_θ and the voltage due to the external network and make the resulting load current zero. This, in turn implies that E_2 is either the sum or difference (in case V_θ and the voltage due to external network are opposed) of the open-circuit voltages of the networks A and B.

This shows that the Thevenin's equivalent network, i.e. V_o and Z_o , is the same whether the load is active or passive. Thus, the Thevenin's theorem is valid for an arbitrary load.

1.9 NORTON'S THEOREM

Norton's theorem provides the dual of Thevenin's theorem. In fact the only variation is that the thevenin's equivalent generator and the series impedance are replaced by an equivalent current generator and a shunt admittance. The replacement is in accordance with the source transformation. The transformed network is called the Norton's equivalent network. The various steps, in obtaining the Norton's equivalent network, are shown in Fig. 1.25. We now give a formal statement of the theorem.

1.9.1 Statement of Norton's Theorem

A two-terminal linear active network may be replaced by a current source of value I_θ and a shunt admittance Y_θ. The current I is the short-circuit current between the terminals ab; and Y_θ ($= 1/Z_\theta$) is the admittance viewed at the terminals when the sources in the active network, including those due to initial conditions, are made inactive and replaced by their internal impedances.

The Norton's equivalent circuit is obtained from the Thevenin's equivalent circuit with the following relationships:

$$I_\theta = \frac{V_\theta}{Z_\theta}$$

and

$$Y_\theta = \frac{1}{Z_\theta} \qquad (1.12)$$

Sometimes, the two theorems are treated as one and called the Thevenin-Norton Equivalent Network Theorem.

1.9.2 Proof of Norton's Theorem

Norton's theorem can be proved independently. However, here, we shall prove this theorem by using the results of Thevenin's theorem and source transformation.

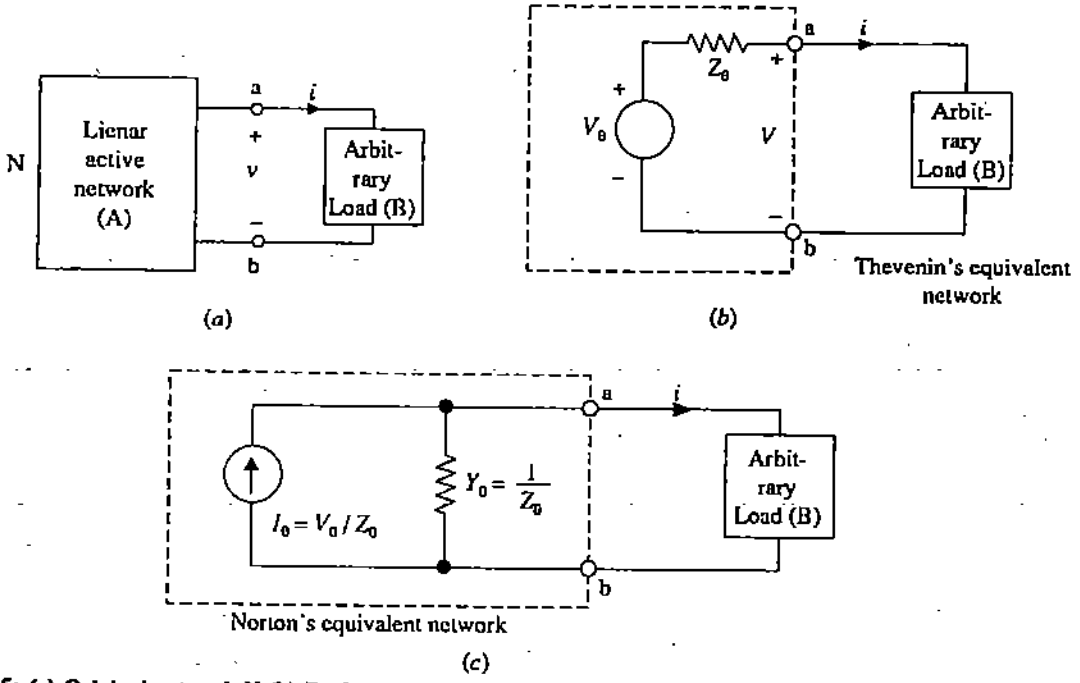


Fig. 1.25: (a) Original network N (b) Replacement of active network A by the Thevenin's equivalent network (c) Replacement of active network by Norton's equivalent network.

Consider the network N of Fig. 1.25.

Its Thevenin's equivalent is obtained as outlined in Section 1.8 ; and the resulting circuit is shown in Fig. 1.25b. Now we transform the Thevenin's equivalent network into a current source. The resulting current generator with shunt impedance is shown within the dotted lines in Fig. 1.25c and satisfies Eq. (1.12). This verify Norton's theorem.

Now, by following an approach similar to the one used for proving Thevenin's theorem, try to prove Norton's theorem independently.

SAQ 5

For the circuit shown in Fig. 1.26 calculate the current in branch a-b when R_{ab} has the following values :

(i) 1 ohm (ii) 5 ohm

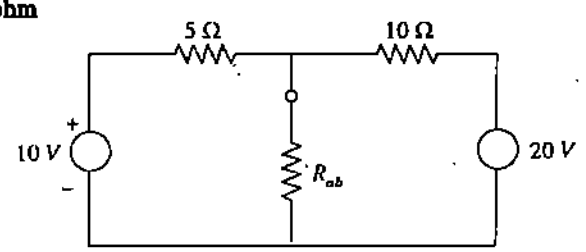


Fig. 1.26: Circuit for SAQ 5.

1.10 MAXIMUM POWER TRANSFER THEOREM

The problem of transferring maximum power to load is of great significance to Electronics and Communication Engineers. We have shown a general system, where V is the energy source, Z is the associated source impedance and Z_l is the load to which the power is to be transferred. In fact, in complicated systems, V and Z represent the Thevenin's equivalent network on the source side. Some examples, of general systems, where maximum power transfer is significant, are broadcasting system, radar and space communication.

1.10.1 Statement and Proof of Maximum Power Transfer Theorem

The optimum load impedance Z_{lm} for the maximum power transfer is equal to the complex conjugate of the source impedance Z_s, i.e.,

$$Z_{lm} = Z_s^* \tag{1.13}$$

Consider the steady state operation of the system shown in Fig. 1.27 at the angular frequency ω of the source V. For simplicity, we shall write Z_l for $Z_l(j)$ and Z_s for $Z_s(j)$.

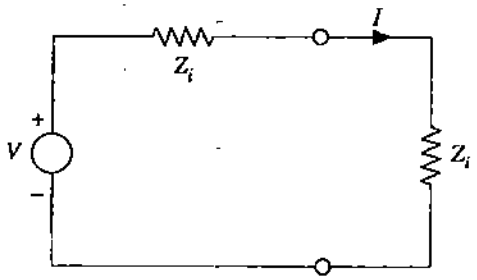


Fig. 1.27: Representation of a general system.

Also, let

$$Z_s = R_s = jX_s$$

and

$$Z_l = R_l = jX_l \tag{1.14}$$

where R_s and R_l are the real parts and X_s and X_l are the imaginary parts of Z_s and Z_l respectively. The average power, delivered to the load, is given by

$$P = [I_s]^2 R_l \tag{1.15}$$

Here the load current is given by

$$I_s = \frac{V_s}{Z_s + Z_l} \tag{1.16}$$

where V_s and I_s are r.m..s. values.

The substitution of I_s in Eq. (1.15) gives

$$P = |V_s|^2 \frac{R_l}{(Z_s + Z_l)^2}$$

$$= |V_s|^2 \frac{R_l}{(R_s + R_l)^2 + (X_s + X_l)^2} \tag{1.17}$$

In this process, we are given V_s, R_s and X_s, and we have to select R_l and X_l so that the power transfer, to the load is maximum. Let us concentrate on the denominator of Eq. (1.17). We first consider the reactive term. It is evident that $(X_s + X_l)^2$ term will become zero when $X_l = -X_s$. This implies that, if X_s is inductive, then X_l must be capacitive. This choice reduces Eq. (1.17) to

$$P = |V_s|^2 \frac{R_s}{(R_s + R_l)^2} \tag{1.18}$$

Now in order to maximize Eq. (1.18), we determine the partial derivative of P with respect to R_l and equate it to zero, i.e.,

$$\frac{\partial P}{\partial R_l} = 0.$$

On using Eq. (1.18) we have

$$\frac{\partial P}{\partial R_l} = |V_s|^2 \frac{(R_l + R_s)^2 - 2(R_l + R_s)R_l}{(R_l + R_s)^4} = 0$$

On simplification of the above expression, we get

$$R_l = R_s.$$

Therfore, the condition, for the transfer of maximum power, is given by

$$R_l = R_s \text{ and } X_l = -X_s \tag{1.19a}$$

or

$$Z_{lm} = R_s - jX_l = Z_s^* \tag{1.19b}$$

1.11 SUMMARY

- Kirchoff's laws state that :

  (1) In an electric network the algebraic sum of the current at a junction point is zero.

(2) In a closed loop the algebraic sum of the potential difference across each circuit component is zero.

- The superposition theorem is valid only for linear networks. It is useful when the network has a large number of energy sources as it makes possible to consider the effect of each source separately. The theorem states that, in a linear network, the overall response, including the equivalent of initial conditions, is equal to the sum of individual responses of each source considered separately.
- The reciprocity theorem states that in any passive linear; bilateral network containing bilateral linear impedances and sources of emf the ratio of a voltage E introduced in one mesh to the current I in any other mesh is the same as the ratio obtained if the position of E and I are interchanged.
- Thevenin's theorem states that in any two terminal network of fixed resistance and constant sources of emf, the current in a load resistor connected to the output terminals is equal to the current that would exist in the same resistor if it were connected in series with (a) a simple emf whose voltage is measured at the open-circuited network terminals and (b) a simple resistance whose magnitude is that of the network looking back from the two terminals into the network with all the sources of emf replaced by their internal resistance.
- Norton's theorem states that any two-terminal linear network containing energy sources and impedances can be replaced by an equivalent circuit consisting of a current source I in parallel with an admittance Y.
- The maximum power transfer theorem states that the condition for the transmission of maximum power to the load (optimum load matching), is that the load impedance must be the complex conjugate of the source impedance, i.e., $Z = Z_s^*$.

1.12 TERMINAL QUESTIONS

1. In Fig. 1.28, the equivalent circuit of an electronic amplifier is shown. Calculate its output voltage.

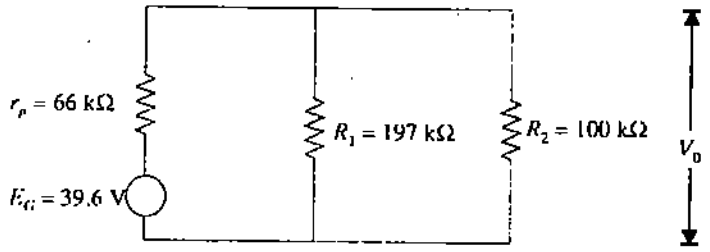


Fig. 1.28:

2. Using superposition theorem, determine the current in the given network shown in Fig. 1.29.

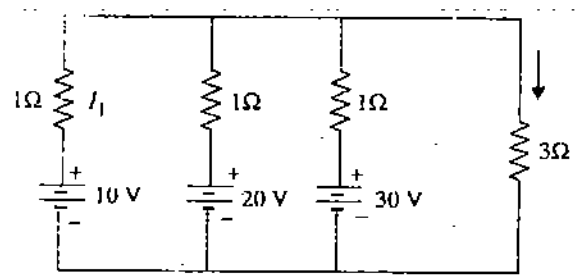


Fig. 1.29:

3. Solve the network shown in Fig. 1.30 for the branch current using Norton's theorem.

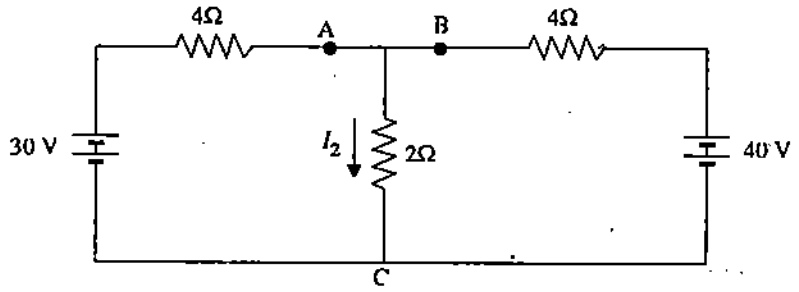


Fig. 1.30:

4. A length of a uniform wire of resistance 10 ohm is bent into a circle and two points at a quarter of the circumference apart are connected with battery of internal resistance 1 ohm and emf 3 volt. Find the current in the different parts of the circuit.

1.13 SOLUTIONS AND ANSWERS

SAQ's

1. Writing KCL at node 1.

$$\frac{10-V}{3}=\frac{V+3}{2}+\frac{V}{1}$$

Solving this gives $V = 1$.

2. For determining the current i_1 due to the current source, we replace voltage source by a short circuit. The corresponding circuit is shown in Fig. 1.31(a) and the current i_1 is given by

$$i_1=\frac{2}{2+R}\times 2=\frac{4}{2+R}$$

For determining the current i_2 due to voltage source, the current source is replaced by open circuit. The corresponding circuit is shown in Fig. 1.31(b) and the current i_2 is given by

$$i_2=\frac{2}{2+R}$$

Applying Superposition theorem we get

$$i_1 + i_2 = i = 1$$

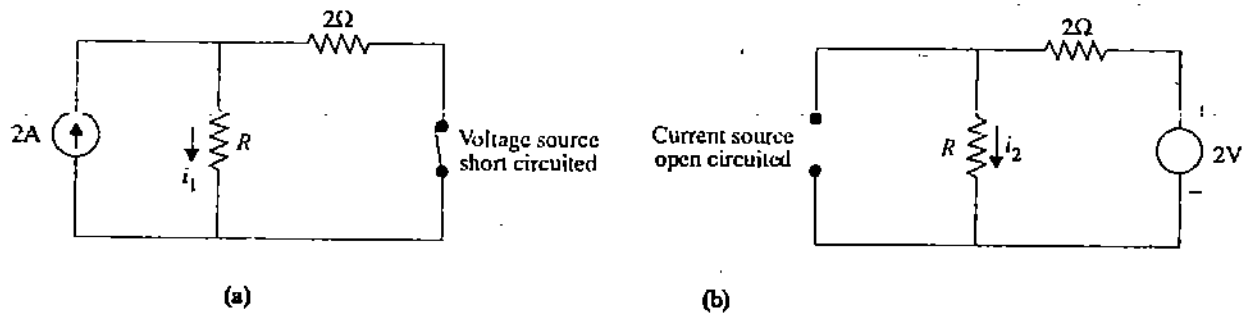


Fig. 1.31:

$$\Rightarrow \frac{4}{2+R}+\frac{2}{2+R}=1$$

$$\Rightarrow \frac{6}{2+R}=1$$

$$\Rightarrow 1=2+R$$

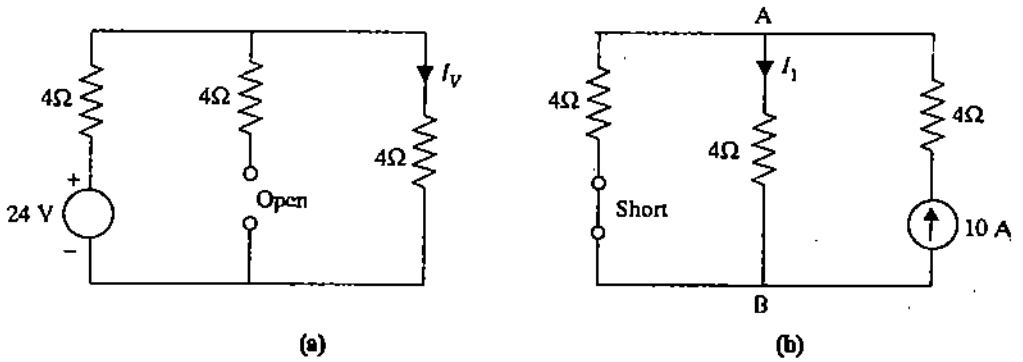
$$\Rightarrow R=4\,\Omega$$

3. Let us first consider the response due to the voltage source when the current source is rendered inoperative by open-circuiting it. The resulting circuit is shown in Fig. 1.32(a). The current I_v, due to the voltage source, is

$$I_v=\frac{24}{4+4}=3\text{ A}$$

For determining the response only due to the current source, we replace the voltage source by a short-circuit. The corresponding circuit is shown in Fig.1.32(b) and the current in AB is

$$I_i=10\frac{4}{4+4}=5\text{ A}$$



(a) (b)

Fig. 1.32: Circuit after making (a) current source inoperative (b) voltage source inoperative.

Now applying superposition principle, we have

$$I=I_v+I_i=8\text{ A}$$

(We urge you to verify the result by the Nodal analysis).

4. The branch current I, I_1 and I_2 are :

$$I=\frac{20}{4}=5\text{ A}$$

$$I_1=\frac{20}{2}=10\text{ A}$$

and

$$I_2=\frac{20}{5}=10\text{ A}$$

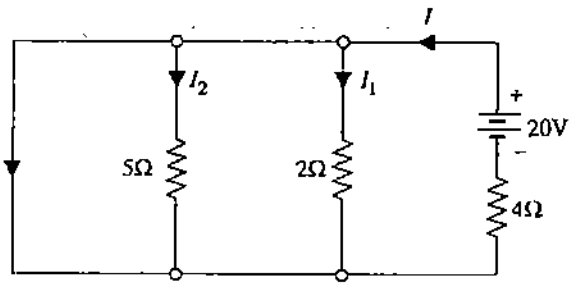


Fig. 1.33

For the verification of reciprocity theorem, we replace the original source by a short-circuit and introduce an equivalent source in the branch containing the 4 ohm resistor. The resulting circuit is shown in Fig. 1.33. The total current, drawn from the battery, is

$$I_T = \frac{20}{4} = 5 \text{ A}.$$

Now all the current will pass through the short-circuit, i.e.

$$I' = 5 \text{ A}$$

and

$$I_1 = I_2 = 0 \text{ A}.$$

As $I' = I = 5$ A, the reciprocity theorem is verified. Also, the changes, in currents in the 5- and 2-ohm resistors, are from 4A and 10A, respectively to zero amp (each).

5. We solve the problem by using Norton's theorem. The resistor R_{ab} is assumed to be the load and we determine the Norton's equivalent of the remaining circuit.

The current I_θ is obtained by finding the current in the short-circuit placed between points a and b. Therfore, from Fig. 1.34(a) we have

$$I_\theta = I_{ab} = \frac{10}{5} + \frac{20}{10} = 4 \text{ A}$$

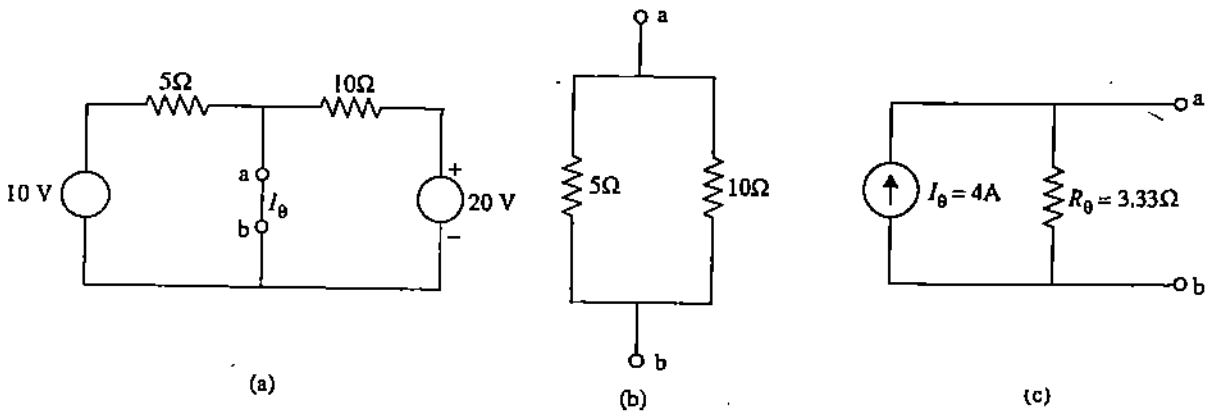


Fig. 1.34: Resulting Circuits at various steps in the analysis of SAQ 5.

We next calculate the resistance R_θ across the terminals a-b, after making the voltage sources inoperative by replacing them with short-circuits. The resulting circuits shown in Fig. 1.34(b). Now, we have

$$R_\theta = R_{ab} = \frac{5 \times 10}{15} = 3.33 \text{ ohm}$$

The Norton's equivalent network, along with the load, is shown in Fig. 1.34(c).

The current in the branch a-b is given by

$$I_{ab} = I_\theta \frac{R_\theta}{R_\theta + R_{ab}}$$

(i) When $R_{ab} = 1$ ohm.

$$I_{ab} = \frac{4 \times 3.33}{3.33 + 1.0} = \frac{4 \times 3.33}{4.33} = 3.076 \text{ A}.$$

(ii) When $R_{ab} = 5$ ohm.

$$I_{ab} = \frac{4 \times 3.33}{3.33 + 5.0} = \frac{4 \times 3.33}{8.33} = 1.6\,\text{A}.$$

Answer of TQs

1. In this problem, We are required to calculate the voltage at the output of the amplifier. As a first step, we replace the voltage source E_p and the series resistor r_p by an equivalent current generator, shown in Fig. 1.35. The current of the equivalent source is

$$I = \frac{E_p}{r_p} = \frac{39.6}{66 \times 10^3}\,\text{A} = 0.6\,\text{mA}.$$

As the three resistances are in parallel after the source trasformation. The equivalent resistance is given by

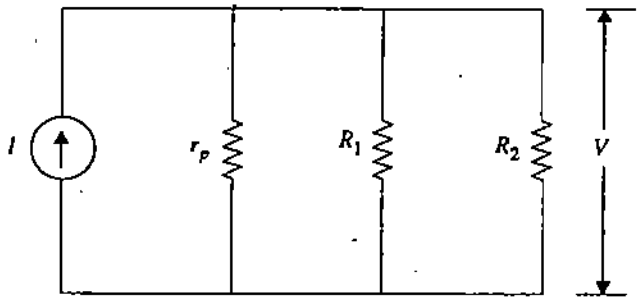


Fig. 1.35:

$$\frac{1}{R_{eq}} = \frac{1}{r_p} + \frac{1}{R_1} + \frac{1}{R_2}$$

On substituting the values and simplification, we get

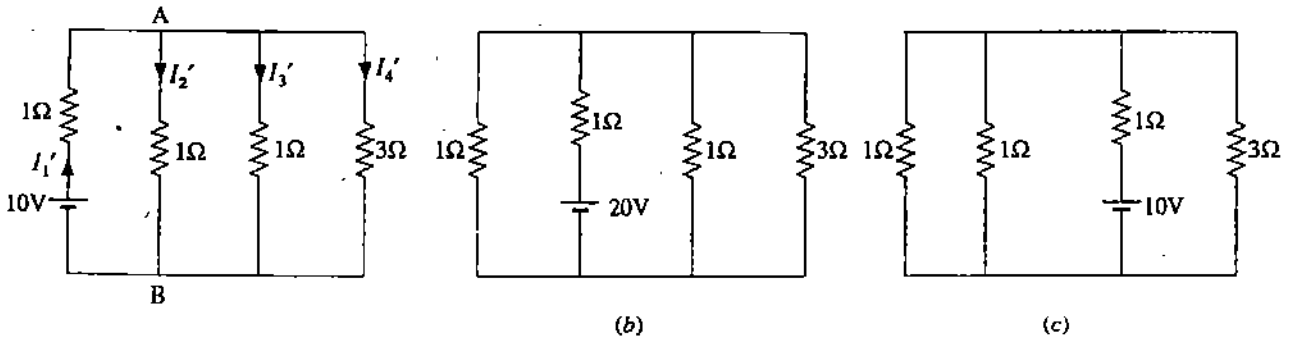
$$R_{eq} = 31.2\,\text{k}\Omega$$

The output voltage is

$$V_o = 0.6 \times 10^{-3} \times 31.2 \times 10^3$$

i.e., $$V_o = 18.72\,\text{volts}$$

2. Superposition theorem for three emf are as follow :



(b) (c)

Fig. 1.36: (a) First emf, (b) second emf, (c) Third emf.

the resistance between the point A and B is given as

$$\frac{1}{R_{AB}} = \frac{1}{1} + \frac{1}{1} = \frac{1}{3} = 2.33$$

$$R_{AB} = 0.429\,\Omega$$

The equivalent resistance across 10V battery in Fig. 1.36(a) is given as

$$R_T = 1 + R_{ab} = 1 + 0.429 = 1.429$$

using ohm's law, we can calculate current

$$I_1' = \frac{10}{R_T} = \frac{10}{1.429} = 7 \text{ A}$$

The voltage drop across AB is

$$V_{AB} = I_1' R_{AB} = 7.00 \times 0.429 = 3 \text{ V}$$

The branch currents in Fig. 1.36(a) are

$$I_2' = \frac{3}{1} = 3 \text{ A}$$

$$I_3' = \frac{3}{1} = 3 \text{ A}$$

$$I_4' = \frac{3}{3} = 1 \text{ A}$$

Similarly we can calculate the branch Current in Fig. 1.36(b). The branch current in Fig. 1.36(b) are

$$I_1'' = 6 \text{ A}$$

$$I_2'' = 14 \text{ A}$$

$$I_3'' = 6 \text{ A}$$

$$I_4'' = 2 \text{ A}$$

and the branch current in Fig. 1.36(c) can be calculated in similar way, which will be as follows:

$$I_1''' = 12 \text{ A}$$

$$I_2''' = 12 \text{ A}$$

$$I_3''' = 30 \text{ A}$$

$$I_4''' = 6 \text{ A}$$

From the above equation, we get

$$I_1 = I_1' - I_1'' - I_1''' = 7 - 6 - 12 = -11 \text{ A}$$

$$I_2 = -I_2' + I_2'' + I_2''' = -3 + 14 - 12 = -1 \text{ A}$$

$$I_3 = -I_3' - I_3'' + I_3''' = -3 - 6 + 30 - 21 \text{ A}$$

$$I_4 = I_4' + I_4'' + I_4''' = I + 2 + 6 = 9 \text{ A}$$

3. The Norton's equivalent is given by Fig. 1.37

$$I = 7.5 + 10 = 17.5 \text{ A}$$

$$\frac{1}{R} = \frac{1}{4} + \frac{1}{2} + \frac{1}{4} = 1 \quad \therefore \quad R = 1 \Omega$$

$$I_2 = \frac{17.5}{2} = 8.75 \text{ A}$$

The voltage drop from C to A is 30 - 17.5 = 12.5 V. Then

$$30 - 17.5 = 12.5 \text{ V}$$

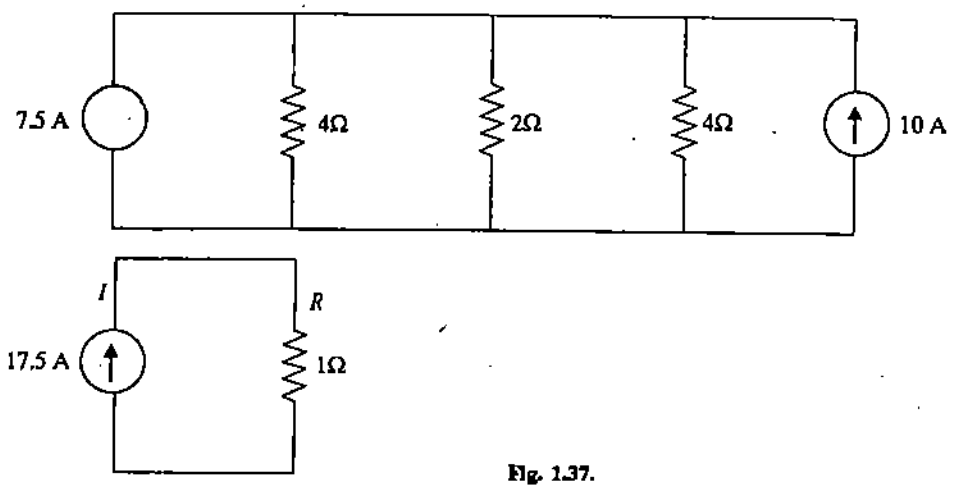


Fig. 1.37.

$$I_1 = \frac{12.5}{4} = 3.125\,\text{A}$$

and the voltage drop from C to B is 40 – 17.5 is 22.5 V. Then I_3 is given by

$$I_3 = \frac{22.5}{4} = 5.625\,\text{A}$$

4. See fig. 1.38 total resistance of the wire ABC = 10 ohm

Resistance of the portion AB, $r_1 = 10 \times \frac{1}{4} = 2.5$ and resistance of the portion ABC,

$$r_2 = 10 \times \frac{3}{4} = 7.5\,\Omega$$

These two resistance r_1 and r_2 are in parallel. Therefore their resultant resistance R is given by

$$\frac{1}{R} = \frac{1}{r_1} + \frac{1}{r_2} = \frac{1}{2.5} + \frac{1}{7.5}$$

$$= \frac{10}{2.5 \times 7.5} = \frac{8}{15}$$

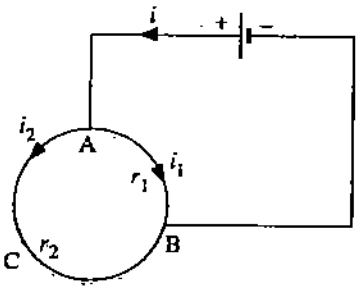


Fig. 1.38.

$$R = \frac{15}{8}\,\text{ohm}$$

Internal resistance of battery

$$r_3 = 1\,\text{ohm}$$

Total resistance in the circuit

$$R_T = R + r_3$$

$$R_T = \frac{15}{8} + 1 = \frac{23}{8} \text{ ohm}$$

Total current $i = \frac{V}{R_T} = \frac{3 \times 8}{23} = \frac{24}{23}$ A

Let the currents in the portion AB and ACB be i_1 and i_2 respectively. The potential difference between A and B is $V_A - V_B$

$\therefore \quad V_A - V_B = r_1 \times i_1 = r_2 i_2$

$\therefore \quad 2.5 i_1 = 7.5 i_2$ or $i_1 = 3i_2$

But $i_1 + i_2 = i = \frac{24}{23}$ A

$\therefore \quad 3i_2 + i_2 = \frac{24}{23}$

or, $i_2 = \frac{24}{23} \times \frac{1}{4} = \frac{6}{23}$ A

$i_1 = 3i_2 = \frac{18}{23}$ A.

UNIT 2 A.C. AND D.C. CIRCUITS

Structure

2.1 INTRODUCTION

In this unit you will study the practical application of some circuits of passive elements. The most important among these are resonant circuits. The series resonant circuits are used to offer a low impedance and the parallel resonant circuit to offer high impedance at a desired frequency. In every day life we see that by moving a knob in a transistor radio we can get the programme from a desired station. This is achieved by filters, which allows to select desired frequencies from a signal (source) having wide range of frequencies. In order to reduce or stop power at the output at desired frequencies without loosing power in the circuit (reactive elements) we use attenuators. We have learnt in maximum power transfer theorem, that the maximum power from a source to a load is transferred when certain impedance conditions are satisfied (matched impedance). It is not always possible to have a source and a load to which power has to be delivered satisfy the matched impedance conditions. This is achieved by using special impedance matching circuit so that the source at its output sees a matched impedance and the load to which power has to be delivered sees a matched impedance at its input. Resonant circuits, filters, attenuators and impedance matching circuits find applications in Instrumentation, telemetering equipment etc., where it is necessary to transmit or attenuate a limited range of frequencies. The topics of this unit, find wide applications in communication world and hence are very important.

Objectives

After going through this unit, you will be able to

- explain complex impedance,

- describe resonance phenomenon in series and parallel resonant circuits,
- explain concept of impedance matching,
- explain characterisics of low pass, high pass and band pass filters and their designs, and
- describe attenuators.

2.2 RECALL COMPLEX IMPEDANCE

You have already learned that in the resistive element, there is no phase difference between the voltage and current whereas in case of pure inductors, the voltage leads over current by $\pi/2$ and in pure capacitors, the voltage lags behind the current by $\pi/2$. Almost all the electric circuits offer impedance to the flow of current. Impedance is the vector sum of Inductive reactance, capacitative reactance and resistance.

Consider the *RL* series circuit shown in Fig.2.1. If we apply the real function $V_m \cos \omega t$ to the circuit, the response may be $I_m \cos \omega t$. Similarly, if we apply

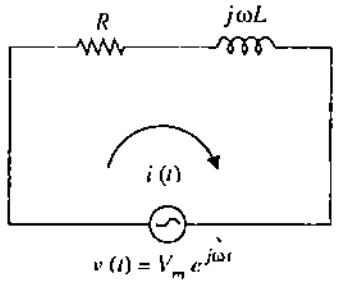


Fig. 2.1: Series *RL* network.

imaginary function $jV_m \sin \omega t$ to the same circuit, the response will be $j\, I_m \sin \omega t$. If we apply a complex function, which is the combination of real and imaginary functions, we will get the complex response. The complex function is $V_m\, e^{j\omega t} = V_m$ ($\cos \omega t + j \sin \omega t$). Applying KVL (Kirchoff's Voltage Law) to the circuit shown in Fig. 2.1, we get

$$V_m e^{j\omega t} = R\, i(t) + L\left(\frac{di}{dt}\right)$$

This is a first order linear differential equation with constant coefficient and can be easily solved. The simplest way to solve is to choose a trial solution for $i(t)$ as :

$$i(t) = I_m e^{j\omega t}$$

If this happens to be a solution of the differential equation, then it must satisfy it completely. By substituting, we get

$$V_m e^{j\omega t} = R I_m e^{j\omega t} + L I_m\, j\omega e^{j\omega t}$$

$$\therefore \quad V_m = (R + j\omega L)\, I_m$$

$$\therefore \quad I_m = \frac{V_m}{(R + j\omega L)}$$

$$\therefore \quad i(t) = I_m e^{j\omega t} = \frac{V_m}{(R + j\omega L)} e^{j\omega t}$$

Impedance is defined as the ratio of voltage to current as follows :

$$Z = \frac{v(t)}{i(t)} = \frac{V_m e^{j\omega t}}{I_m e^{j\omega t}} = R + j\omega L$$

Complex impedance (Z) is the total opposition offered by the circuit elements to ac current and can be displayed on the complex plane. In the expression for Z, the resistance R is the real part of the impedance, and the reactance X_L is the imaginary part of the impedance. The resultant of R and X_L is called the complex impedance as shown in Fig. 2.2. This is called impedance diagram. From Figure, it is clear that

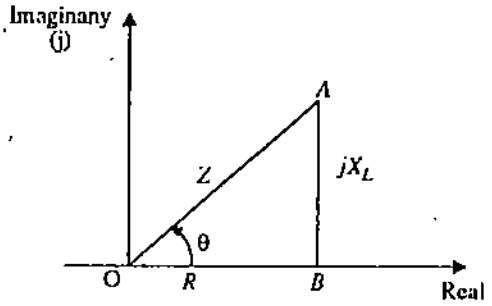


Fig. 2.2: Impedance diagram of *RL* network.

$|Z| = \sqrt{R^2 + (\omega L)^2}$ and angle $\theta = \tan^{-1}\left(\frac{\omega L}{R}\right)$. Here, impedance is the vector sum of resistance and inductive reactance.

$$Z = R + j\omega L$$

$$= |Z| \angle Z$$

Where $$|Z| = \sqrt{R^2 + \omega^2 L^2}$$

and $$\angle Z = e^{j\tan^{-1}\left(\frac{\omega L}{R}\right)}$$

This can be deduced as follows :

Let $$R = A\cos\theta$$

and $$\omega L = A\sin\theta$$

Squaring & adding, we get

$$R^2 + \omega^2 L^2 = A^2 (\cos^2\theta + \sin^2\theta)$$

$$A = \sqrt{R^2 + \omega^2 L^2}$$

also, $$\frac{A\sin\theta}{A\cos\theta} = \frac{\omega L}{R} \Rightarrow \theta = \tan^{-1}\left(\frac{\omega L}{R}\right)$$

Clearly, $Z = A(\cos\theta + j\sin\theta) = A e^{j\theta}$

$$= \sqrt{R^2 + \omega^2 L^2}\, e^{j\tan^{-1}\left(\frac{\omega L}{R}\right)} = |Z| \angle Z$$

Similarly, if we consider *RC* series circuit, as shown in Fig. 2.3, and apply complex voltage $v(t) = V_m e^{j\omega t}$, we get, complex response as shown below : Applying KVL in the circuit shown we get,

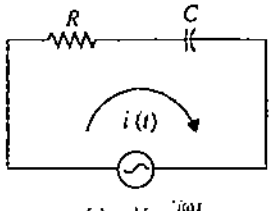


Fig. 2.3: Series *RC* network.

$$V_m e^{j\omega t} = Ri(t) + \frac{1}{C}\int i(t)\,dt$$

As $v - i$ relation for capacitor is given by

$$i(t) = C\frac{dv_c(t)}{dt}$$

$$\rightarrow \quad v_c(t) = \frac{1}{C}\int i(t)\,dt$$

Taking trial solution of the above equation as

$i(t) = I_m e^{j\omega t}$ we get

$$V_m e^{j\omega t} = RI_m e^{j\omega t} + \frac{1}{C} I_m \left(\frac{1}{j\omega}\right) e^{j\omega t} = \left[RI_m - \frac{j}{\omega C} I_m\right] e^{j\omega t}$$

$$\rightarrow V_m = \left(R - \frac{j}{\omega C}\right) I_m \rightarrow I_m = \frac{V_m}{(R - j/\omega C)}$$

$$\therefore \quad i(t) = \frac{V_m}{(R - j/\omega C)} e^{j\omega t} = \frac{v(t)}{(R - j/\omega C)}$$

$\therefore$ The impedance $Z = \dfrac{v(t)}{i(t)} = R \ -j/\omega C$

Here, the impedance Z consists of resistance (R), which is real part, and capacitive reactance $X_C = \dfrac{1}{\omega C}$ which is imaginary part of the impedance. The impedance diagram is shown in Fig. 2.4. From this diagram, the impedance

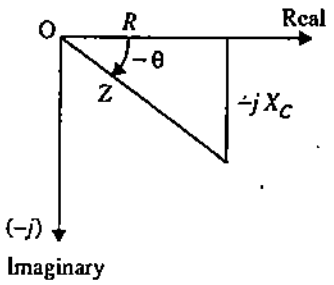


Fig. 2.4: Impedance diagram for series *RC* network.

$$|Z| = \sqrt{R^2 + X_C^2}$$

$$= \sqrt{R^2 + \frac{1}{\omega^2 C^2}}$$

and angle $\theta = \tan^{-1}\left(\dfrac{1}{\omega CR}\right)$

Also, we can write,

$$Z = R - \frac{j}{\omega C}$$

$$= \sqrt{R^2 + \frac{1}{\omega^2 C^2}} \ e^{j\tan^{-1}\left(-\frac{1}{\omega CR}\right)}$$

Example 1. In a circuit, consisting of 1 kΩ resistor connected in series with 50 mH coil, a 10V rms, 10 kHz signal is applied. Find impedance Z, current I, phase angle θ, V_R and V_L.

Solution. $R = 1\ \text{k}\Omega = 1000\ \Omega$

$$X_L = \omega L = 2\pi f L$$

$$= 6.28 \times 10 \times 10^3 \times 50 \times 10^{-3}$$

$$= 3140\ \Omega$$

$$\therefore \quad Z = R + j\omega L = 1000 + j\,3140$$

$$|Z| = \sqrt{(1000)^2 + (3140)^2} = 3295.4\ \Omega$$

Current $I_{rms} = \dfrac{V_{rms}}{Z} = \dfrac{10}{3295.4} = 3.03\ \text{mA}$

phase angle $(\theta) = \tan^{-1}\left(\dfrac{\omega L}{R}\right) = \tan^{-1}\left(\dfrac{3140}{1000}\right) = 72.33^\circ$

$$V_R = I_{rms}\, R = 3.30 \times 10^{-3} \times 1000 = 3.03\ \text{V}$$

$$V_L = I_{rms}(\omega L) = 3.02 \times 10^{-3} \times 3140 = 9.51\ \text{V}$$

Example 2. A sine wave generator supplies a 500 Hz, 10 V_{rms} signal to a 2 kΩ resistor in series with a 0.1 μF capacitor as shown in Fig. 2.5. Determine the total impedance Z, current I, phase angle θ, capacitive voltage V_C, and resistive voltage V_R.

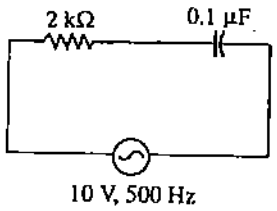


Fig. 2.5

Solution. $X_C = \dfrac{1}{2\pi f C} = \dfrac{1}{2 \times 3.14 \times 14 \times 500 \times 0.1 \times 10^{-6}}$

$$= 3184.7\ \Omega$$

Total impedance $Z = R + \dfrac{1}{j\omega C} = R - \dfrac{j}{2\pi f C} = R - j\,X_C$

$$= (2000 - j\,3184.71)\ \Omega$$

$$\therefore \quad |Z| = \sqrt{(2000)^2 + (3184.7)^2} = 3760.6\ \Omega$$

Phase angle $(\theta) = \tan^{-1}\left(\dfrac{-1}{R\omega C}\right) = \tan^{-1}\left(\dfrac{-X_C}{R}\right)$

$$= -\tan^{-1}\left(\frac{3184.7}{2000}\right) = -57.87^\circ$$

Current $(I) = \dfrac{V_{rms}}{|Z|} = \dfrac{10}{3760.0} = 2.66\ \text{mA}$

Capacitive voltage, $V_C = I\,X_C = 2.66 \times 10^{-3} \times 3184.7 = 8.47\ \text{V}$

Resistive voltage, $V_R = IR = 2.66 \times 10^{-3} \times 2000 = 5.32\ \text{V}$

Remarks : You must have noted that the arithmetic sum of V_C and V_R does not give the applied voltage (10V). In fact, the total applied voltage is a complex quantity

given by

$$V_S = (5.32 - j\,8.47)\ \text{V} = 10 \angle -57.87^\circ\ \text{V}$$

SAQ 1

Determine the source voltage and the phase angle, if the voltage across the resistance is 70V and the voltage across the inductive reactance is 20V as shown in Fig. 2.6.

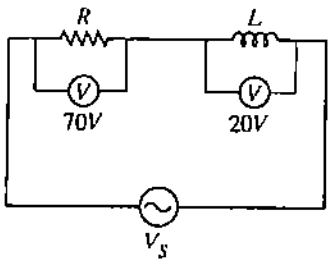


Fig. 2.6

SAQ 2

Determine the source voltage and phase angle when the voltage across the resistor is 20V and the voltage across the capacitor is 30V as shown in Fig. 2.7.

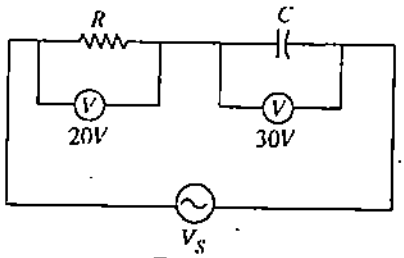


Fig. 2.7

2.3 RESONANT CIRCUITS

We call a circuit a resonant circuit if at a particular frequency called resonant frequency the capacitive reactance X_C and inductive reactance X_L are equal i.e., $X_L = X_C$. In many of the electrical circuit, resonance is a very important phenomenon. The study of resonance is very useful, particularly in the area of communications. For example, the ability of a radio-receiver to select a certain frequency, transmitted by a station and to eliminate frequencies from other stations is based on the principle of resonance. In this section we will study the essential features of series and parallel resonant circuit.

2.3.1 Series Resonant Circuit

In a series *RLC* circuit, the current lags behind, or leads the applied voltage depending upon the values of X_L and X_C. X_L causes the total current to lag behind the applied voltage, while X_C causes the total current to lead over the applied voltage. When $X_L > X_C$, the circuit is predominantly inductive and when $X_C > X_L$, the circuit is predominantly capacitive. However, if one of the parameters of the series *RLC* circuit is varied in such a way that the current is in phase with the applied voltage, then the circuit is said to be in "resonance". Consider a series *RLC* circuit shown in Fig. 2.8. The total impedance for the series *RLC* circuit is :

$$Z = R + j\omega L + \frac{1}{j\omega C} = R + j\omega L - \frac{j}{\omega C}$$

$$= R + jX_L - j\,X_C = R + j\,(X_L - X_C)$$

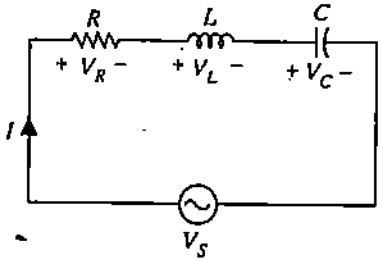


Fig. 2.8: Series *RLC* circuit.

$$= R + j\left(\omega L - \frac{1}{\omega C}\right)$$

The circuit is said to be in resonance if the current is in phase with the applied voltage. In a series *RLC* circuit, "resonance" occurs when $X_L = X_C$. The frequency at which the resonance occurs is called the "resonant frequency". When $X_L = X_C$, the impedance in a series *RLC* circuit is purely resistive. At resonant frequency (f_0), the voltages across capacitance and inductance are equal in magnitude. Since they are 180° out of phase with each other, they cancel each other, hence, zero voltage appears across the *LC* combination.

At resonance, $X_L = X_C$

i.e. $\omega L = \frac{1}{\omega C}$

$$\rightarrow 2\pi f_0 L = \frac{1}{2\pi f_0 C}$$

$$\rightarrow f_0^2 = \frac{1}{4\pi^2 LC}$$

$$\rightarrow f_0 = \frac{1}{2\pi\sqrt{LC}}$$

In a series *RLC* circuit, the resonance may be produced by varying the frequency, keeping L and C constant, otherwise resonance may be produced by varying either L or C for a fixed frequency.

2.3.2 Impedance and Phase Angle of a Series Resonant Circuit

As we have already seen in previous section, the impedance of a series *RLC* circuit is given by :

$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right)$$

$$= \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}\; e^{j\tan^{-1}\frac{\left(\omega L - \frac{1}{\omega C}\right)}{R}}$$

Here $|Z| = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} = \sqrt{R^2 + (X_L - X_C)^2}$

The variation of X_L, X_C and Z with frequency is shown in Fig. 2.9. At zero frequency, both X_C and Z are infinitely large and X_L is zero because the capacitor acts as open circuit at zero frequency. As the frequency increases, X_C decreases and X_L increases. Since X_C is larger than X_L at frequencies below the resonant frequency (f_0), Z decreases along with X_C. At resonant frequency (f_0), $X_C = X_L$ and $Z = R$. At frequencies above the resonant frequency, X_L is larger than X_C causing Z to increase.

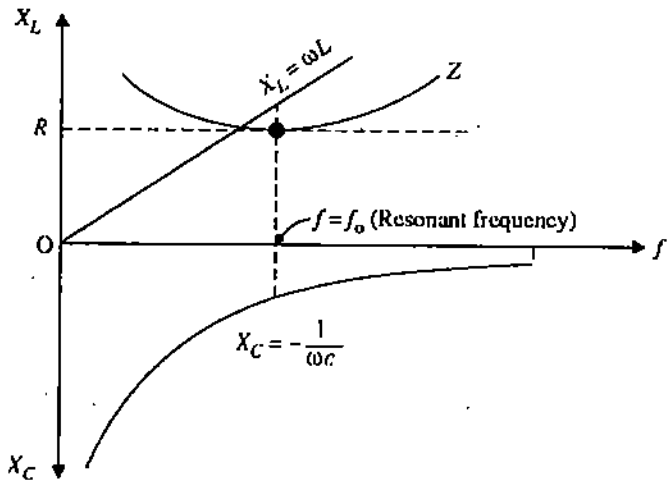


Fig. 2.9: Variation of X_L, X_C and Z with frequency.

The phase angle associated with total impedance in series *RLC* circuit is given by :

$$\phi = \tan^{-1} \frac{\left(\omega L - \frac{1}{\omega C}\right)}{R}$$

The variation of phase angle with frequency is shown in Fig. 2.10 At a frequency

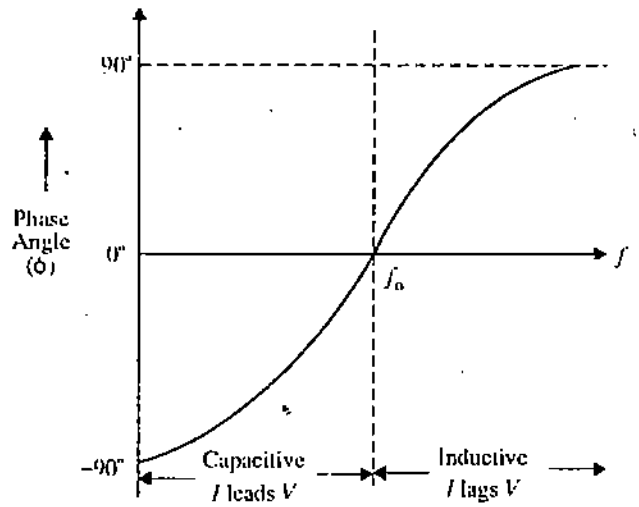


Fig. 2.10: Variation of phase angle with frequency.

below the resonant frequency, the current leads over source voltage because the capacitive reactance is greater than the inductive reactance. The phase angle decreases as the frequency approaches the resonant value, and is 0° at resonance. At frequencies above resonance, the current lags behind the source voltage, because the inductive reactance is greater than capacitive reactance. As the frequency goes higher, the phase angle approaches + 90°.

2.3.3 Voltages and Current in a Series Resonant Circuit

We know, in a series *RLC* network

$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right) = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}\; e^{j\tan^{-1}\frac{\left(\omega L - \frac{1}{\omega C}\right)}{R}}$$

$$|Z| = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}$$

$$I = \frac{V_0}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}}$$

Where V_0 and I are amplitude of voltage and current respectively. The variation of impedance and current with frequency is shown in Fig. 2.11. As we have learned in

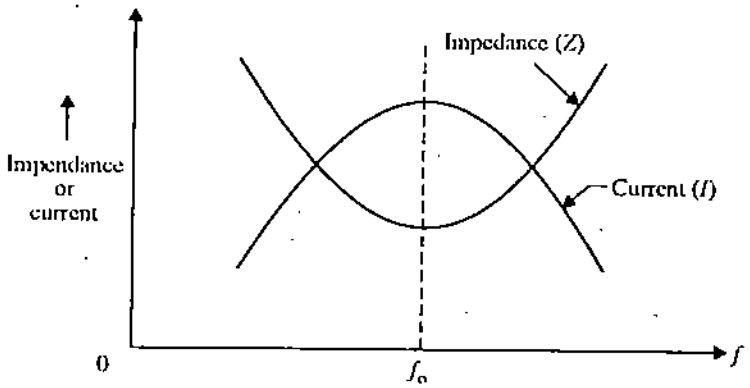


Fig. 2.11: Variation of impedance and current with frequency.

previous sections, at resonant frequency, the capacitive reactance is equal to inductive reactance, and hence the impedance is minimum. Because of the minimum impedance, maximum current flows through the circuit. This value of current is given by

$$I_0 = \text{current at resonant frequency} = \frac{V_0}{R}$$

The voltage drop across resistance, inductance and capacitance also varies with frequency. At $f = 0$, the capacitor acts as an open circuit and blocks current. Hence, complete source voltage appears across the capacitor. As the frequency increases, X_C decreases and X_L increases, causing total reactance $(X_C - X_L)$ to decrease. As a result, the impedance decreases and the current increases. As current increases, voltage drop across resistance, inductance and capacitance (V_R, V_L & V_C) also increases. When the frequency becomes equal to the resonant frequency (f_0), the impedence is equal to resistance (R) and hence current reaches its maximum value and V_R is also of maximum value. At this frequency, the voltage drop across capacitance and inductance are equal in magnitude and opposite in phase. As the frequency is increased further, X_L continues to increase and X_C continues to decrease, causing the total reactance $(X_L - X_C)$ to increase. As a result, there is decrease in current. If the frequency is increased still further, the current approaches zero, both V_R and V_C approaches zero and V_L approaches V_0. The response of different voltage with frequency is shown in Fig. 2.12.

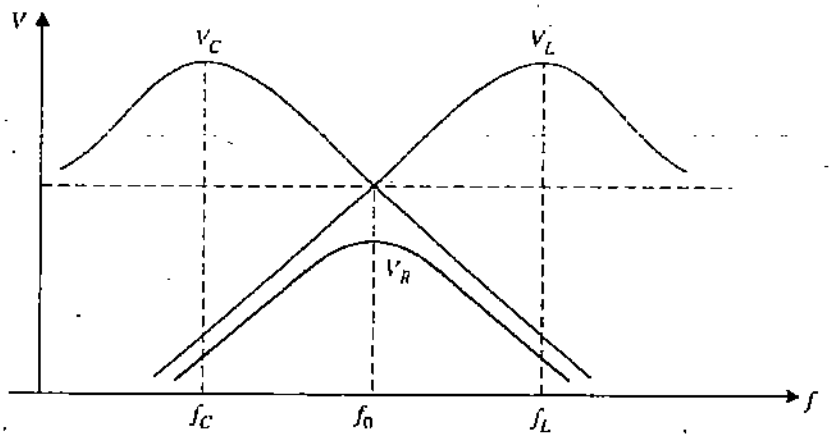


Fig. 2.12: Variation of V_C, V_L and V_R with frequency.

2.3.4 Band Width of a RLC Circuit

The band width of any system is defined as the range of frequencies for which the current or output voltage is equal to 70.7% of its peak value at the resonant frequency. Fig. 2.13 shows the frequency response of a series *RLC* circuit. Here the

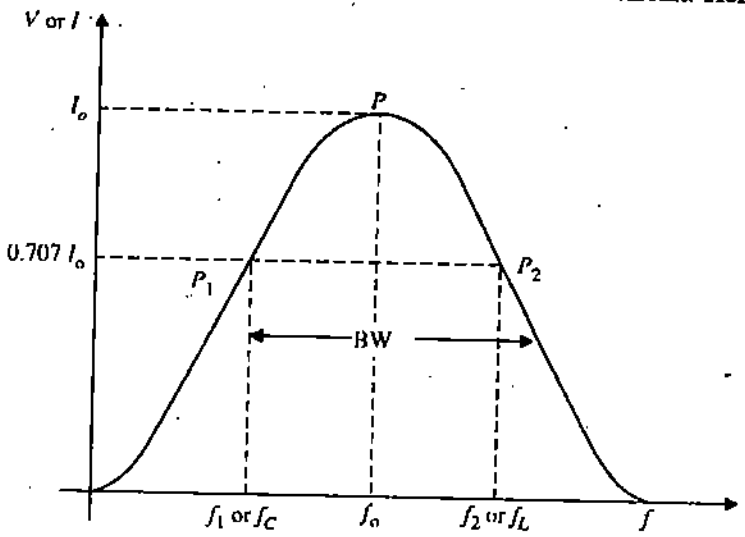


Fig. 2.13: Frequency response of RLC network.

frequency f_1 is the frequency at which the current is 0.707 times the current at resonant value, and it is called the lower cut off frequency. The frequency f_2 is the frequency at which the current is 0.707 times the current at resonant value and is called the upper cut off frequency. The band width (BW) is defined as :

$$BW = (f_2 - f_1)\,\text{Hz}$$

If the current at P_1 is 0.707 I_0, the impedance of the circuit at this point is $\sqrt{2}R$, and hence

$$\frac{1}{\omega_1 C} - \omega_1 L = R$$

Similarly, $$\omega_2 L - \frac{1}{\omega_2 C} = R$$

Equating these equation, we obtain

$$\frac{1}{\omega_1 C} - \omega_1 L = \omega_2 L - \frac{1}{\omega_2 C}$$

$$(\omega_1 + \omega_2) L = \frac{(\omega_1 + \omega_2)}{(\omega_1\,\omega_2)} \frac{1}{C}$$

$$\rightarrow \omega_1 \omega_2 = \frac{1}{LC}$$

We know, $$\omega_0^2 = \frac{1}{LC}$$

Therefore, $$\omega_0^2 = \omega_1 \omega_2$$

Adding equations for R, we get

$$\frac{1}{\omega_1 C} - \omega_1 L + \omega_2 L - \frac{1}{\omega_2 C} = 2R$$

$$\rightarrow (\omega_2 - \omega_1) L + \frac{(\omega_2 - \omega_1)}{\omega_2 . \omega_1} \frac{1}{C} = 2R$$

Since $\omega_0^2 = \frac{1}{LC} \rightarrow C = \frac{1}{\omega_0^2 L}$

Substituting these values, we obtain

$$\omega_2 - \omega_1 = \frac{R}{L}$$

$$\rightarrow (f_2 - f_1) = \frac{R}{2\pi L}$$

$$\therefore \quad \text{BW (Band width)} = \frac{R}{2\pi L}$$

From Fig.2.13 we have

$$f_2 - f_1 = \frac{R}{2\pi L} \tag{2.1}$$

$$f_0 - f_1 = \frac{R}{4\pi L} \text{ and } f_2 - f_0 = \frac{R}{4\pi L}$$

The lower frequency limit $f_1 = f_0 - \frac{R}{4\pi L}$

The upper frequency limit $f_2 = f_0 + \frac{R}{4\pi L}$

Rearranging Eq. (2.1) (dividing both sides by f_0), we get

$$\frac{f_2 - f_1}{f_0} = \frac{R}{2\pi f_0 L}$$

Here an important property of a coil is defined. It is the ratio of the reactance of the coil to its resistance. This ratio is defined as the Q of the coil. Q is known as Quality factor or figure of merit, and is an indication of the quality of the coil.

$$Q = \frac{X_L}{R} = \frac{2\pi f_0 L}{R}$$

Clearly, $\frac{1}{Q} = \frac{f_2 - f_1}{f_0} = \frac{\Delta f}{f_0}$

$$Q = \frac{f_0}{\Delta f} = \frac{\text{Resonant frequency}}{\text{Band width}}$$

Clearly, a higher value of Q results in a smaller band width and a lower value of Q causes a larger band width.

2.3.5 Parallel Resonance

A parallel RLC network is shown in Fig. 2.14. Parallel resonance occurs when $X_C = X_L$ and the frequency at which this occurs, is called resonant frequency. When $X_C = X_L$, the two branch currents are equal (provided $R_C = R_L$) in magnitude and 180° out of phase with each other. Therefore, the two current cancel each other and the total current is zero. From Fig. 2.14. the total admittance (Y) is:

$$Y = \frac{1}{R_L + j\omega L} + \frac{1}{\left(R_C - \frac{j}{\omega C}\right)}$$

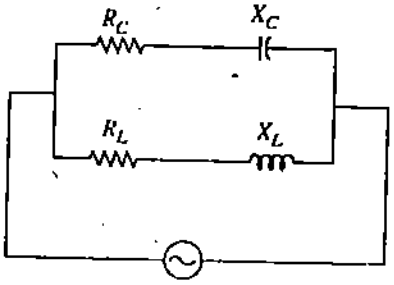


Fig. 2.14: Parallel *RLC* network.

$$= \frac{R_L - j\omega L}{\left(R_L^2 + \omega^2 L^2\right)} + \frac{R_C + j/\omega C}{\left(R_C^2 + \frac{1}{\omega^2 C^2}\right)}$$

$$= \frac{R_L}{(R_L^2 + \omega^2 L^2)} + \frac{R_C}{\left(R_C^2 + \frac{1}{\omega^2 C^2}\right)} + j\left\{\left[\frac{1/\omega C}{R_C^2 + \frac{1}{\omega^2 C^2}}\right] - \left[\frac{\omega L}{R_L^2 + \omega^2 L^2}\right]\right\}$$

At resonance ($\omega = \omega_0$) the imaginary part becomes zero, i.e.,

$$\frac{\omega_0 L}{R_L^2 + \omega_0^2 L^2} = \frac{1/\omega_0 C}{\left(R_C^2 + \frac{1}{\omega_0^2 C^2}\right)}$$

$$\rightarrow \omega_0 L\left[R_C^2 + \frac{1}{\omega_0^2 C^2}\right] = \frac{1}{\omega_0 C}\left[R_L^2 + \omega_0^2 L^2\right]$$

$$\rightarrow \omega_0^2\left[R_C^2 + \frac{1}{\omega_0^2 C^2}\right] = \frac{1}{LC}\left[R_L^2 + \omega_0^2 L^2\right]$$

$$\rightarrow \omega_0^2 R_C^2 - \frac{\omega_0^2 L}{C} = \frac{R_L^2}{LC} - \frac{1}{C^2}$$

$$\rightarrow \omega_0^2\left[R_C^2 - \frac{L}{C}\right] = \frac{1}{LC}\left[R_L^2 - \frac{L}{C}\right]$$

$$\rightarrow \omega_0 = \frac{1}{\sqrt{LC}}\sqrt{\frac{R_L^2 - L/C}{R_C^2 - L/C}}$$

This is general condition for resonance. In special case, when $R_C = R_L$, we get

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

You are advised to determine the resonant circuit for a "tank circuit" shown in

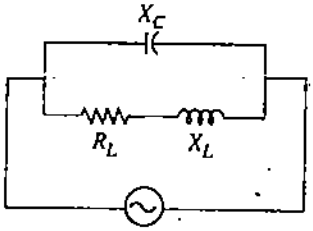


Fig. 2.15: Tank circuit.

Fig. 2.15 and show that the resonant frequency turns out to be

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R_L^2}{L^2}}$$

As you will observe from the expression for impedance (reciprocal of admittance which has been derived), it becomes maximum at the resonant frequency and decreases at lower and higher frequencies as shown in Fig. 2.16 At lower frequencies, X_L is very small and X_C is very large and so the total impedance is essentially inductive. As the frequency increases, the impedance also increases and inductive reactance dominates till the resonant frequency is reached. At this point $X_L = X_C$ and the impedance is at its maximum value. As the frequency goes above the resonance, the capacitive reactance dominates and the impedance decreases as shown in Fig. 2.16.

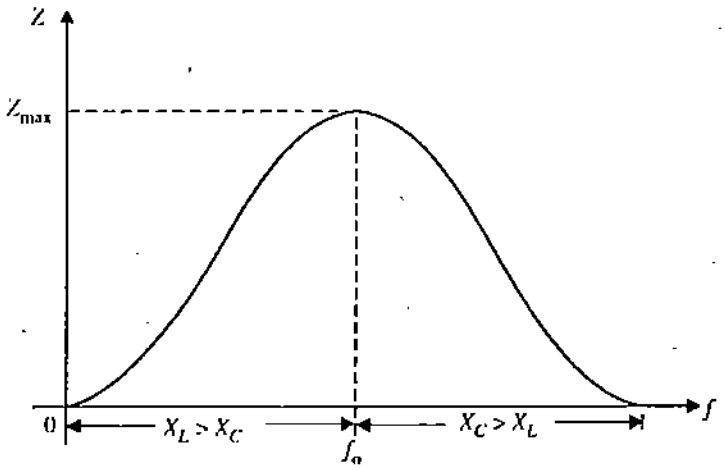


Fig. 2.16: Variation of impedance with frequency.

2.3.6 Q factor of a Parallel Resonant Circuit

Now, let us consider a parallel resonant circuit shown in Fig. 2.17. The total admittance (Y) is

$$Y = G + jB$$

Fig. 2.17: Parallel resonant circuit.

$$Y = \frac{1}{R} + j\omega C + \frac{1}{j\omega L} = \frac{1}{R} + j\left(\omega C - \frac{1}{\omega L}\right)$$

At resonant frequency ($f = f_0$), the imaginary part is zero i.e.,

$$\omega_0 C - \frac{1}{\omega_0 L} = 0$$

$$\Rightarrow \omega_0 = \frac{1}{\sqrt{LC}}$$

$$\Rightarrow f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The voltage and current variation with frequency is shown in Fig. 2.17. Clearly, at resonant frequency, the current is minimum because in parallel resonant circuit, the impedance is maximum.

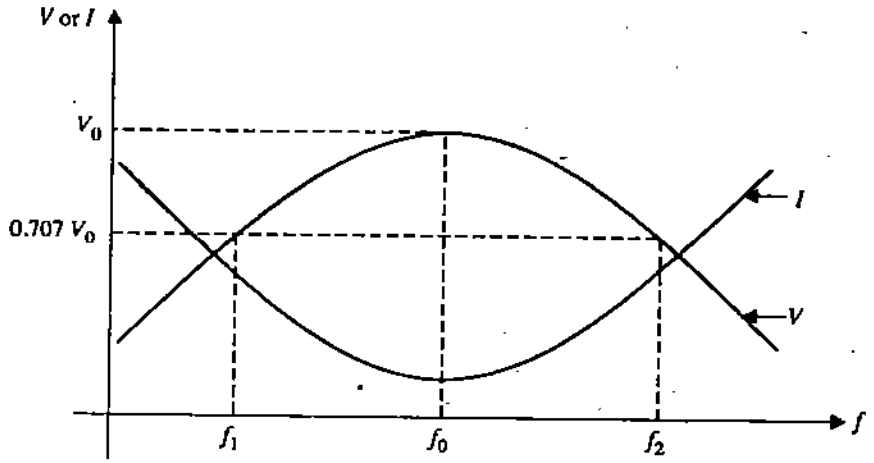


Fig. 2.17: Variation of V and I with frequency in a parallel resonant circuit.

The band width (BW) $= f_2 - f_1$

For, parallel circuit, to obtain the lower cut off frequency (f_1),

$$\omega_1 C - \frac{1}{\omega_1 L} = -\frac{1}{R}$$

$$\omega_1^2 + \frac{\omega_1}{RC} - \frac{1}{LC} = 0$$

$$\rightarrow \quad \omega_1 = -\frac{1}{2RC} + \sqrt{\left(\frac{1}{2RC}\right)^2 + \frac{1}{LC}}$$

Similarly, to obtain upper cut off frequency, (f_2).

$$\omega_2 C - \frac{1}{\omega_2 L} = \frac{1}{R}$$

$$\rightarrow \quad \omega_2 = \frac{1}{2RC} + \sqrt{\left(\frac{1}{2RC}\right)^2 + \frac{1}{LC}}$$

$$\text{BW} = \omega_2 - \omega_1 = \frac{1}{RC}$$

Also, $\quad f_2 - f_1 = \dfrac{1}{2\pi RC}$

The Quality factor $Q = \dfrac{f_0}{f_2 - f_1} = \dfrac{\omega_0}{\omega_2 - \omega_1}$

$$= \frac{\omega_0}{1/RC} = \omega_0 RC$$

Example 3. Determine the resonant frequancey for the circuit shown in Fig. 2.18(a)

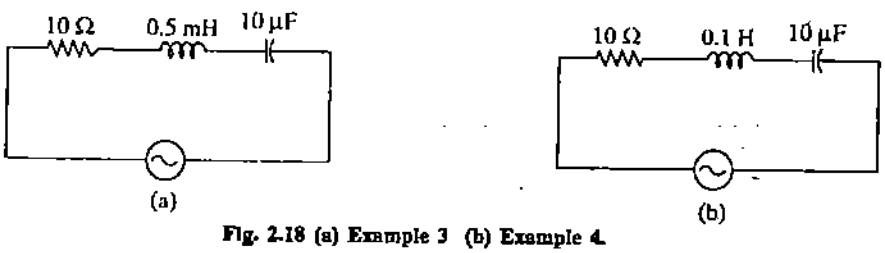


Fig. 2.18 (a) Example 3 (b) Example 4.

Solution : The resonant frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{10\times10^{-6}\times0.5\times10^{-3}}} = 2.25\,\text{KHz}$$

Example 4: For the circuit shown in 2.18 (b) determine the impedance at resonant frequency, 10 Hz above resonant frequency and 10 Hz below resonant frequency.

Solution : At resonant frequency, $X_C = X_L$ and hence total impedance in a series *RLC* resonant circuit is purely resistive.

$$\therefore \quad Z = R = 10\,\Omega \text{ at resonance}$$

Resonant frequency $(f_0) = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.1\times10\times10^{-6}}} = 159.2\,\text{Hz}$

Given, $f_1 = f_0 - 10\text{Hz} = 159.2 - 10 = 149.2\,\text{Hz}$

$$f_2 = f_0 + 10\,\text{Hz} = 159.2 + 10 = 169.2\,\text{Hz}$$

Now, $X_{C_1} = \frac{1}{\omega_1 C} = \frac{1}{2\pi f_1 C} = 106.6\,\Omega$

$$X_{L_1} = \omega_1 L = 2\pi f_1 L = 93.75\,\Omega$$

Also, $X_{C_2} = \frac{1}{\omega_2 C} = \frac{1}{2\pi f_2 C} = 94.06\,\Omega$

$$X_{L_2} = \omega_2 L = 2\pi f_2 L = 106.31\,\Omega$$

Clearly, impedance at $f_1 = 149.2\,\text{Hz}$

$$Z_1 = \sqrt{R^2 + (X_{L_1} - X_{C_1})^2}$$

$$= \sqrt{10^2 + (93.75 - 106.6)^2} = 16.28\,\Omega$$

Here, $X_{C_1} > X_{L_1}$, so Z_1 is capacitive.

And impedance at $_2 = 169.2\,\text{Hz}$

$$Z_2 = \sqrt{R^2 + (X_{L_2} - X_{C_2})^2}$$

$$= \sqrt{10^2 + (106.31 - 94.06)^2)} = 15.81\,\Omega$$

Clearly $X_{L_2} > X_{C_2}$ at this frequency, so Z is inductive in nature.

SAQ 3 In the circuit shown in Fig. 2.19 the inductance of 0.1 H having a Q of 5 is in parallel with capacitor. Determine the value of capacitance and coil resistance at resonant frequency of 500 Hz ?

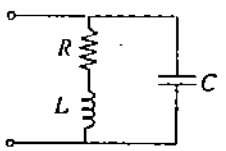


Fig. 2.19:

SAQ 4 A series *RLC* circuit consists of 50 Ω resistance, 0.2 H inductance and 10 μF capacitor with the applied voltage of 20 V. Determine the resonant frequency. Find the Q factor of the circuit. Compute the lower and upper frequency limits and also find the band width of the circuit.

2.4 IMPEDANCE MATCHING

You have already learnt maximum power transfer theorem which states that the maximum power is delivered from source to load when load resistance is equal to the source resistance. It is for this reason that the impedance matching between circuits is so important. As an example, the audio output transformer must match the high impedance of the audio power amplifier and its output to the low input impedance of the speaker. But, maximum power transfer is not always desirable, since the transfer occurs at a 50% efficiency. For many a situations, a maximum voltage transfer is desired, which means that unmatched impedances are necessary. If maximum power transfer is required, the load resistance should be equal to the given source resistance. Maximum power transfer theorem can be applied to complex impedance circuits. If the source impedance is complex then the maximum power transfer occurs when the load impedance is complex conjugate of the source impedance.

Consider a circuit shown in Fig. 2.20 consisting of source impedance delivering power to a complex load. Clearly, the current passing through the circuit is

$$i(t) = \frac{V_s}{(R_s + jX_s) + (R_L + jX_L)}$$

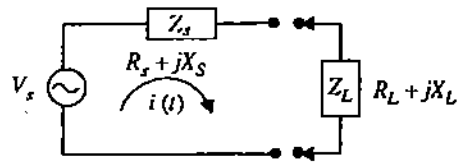


Fig. 2.20: Maximum power transfer for complex load.

The magitude of current $I_0 = |i(t)|$ is given by

$$I_0 = |i(t)| = \frac{V_0}{\sqrt{(R_S + R_L)^2 + (X_S + X_L)^2}}$$

where $V_S = V_0 e^{j\omega t} \rightarrow |V_S| = V_0$

The power delivered to the load is given by

$$P = I_0^2 R_L = \frac{V_0^2 R_L}{\sqrt{(R_S + R_L)^2 + (X_S + X_L)^2}}$$

Clearly, in the above equation, if R_L is kept fixed, the power becomes maximum when

$$X_S = -X_L$$

under this condition, the power is given by

$$P = \frac{V_0^2 R_L}{(R_S + R_L)^2}$$

Now, let us assume that R_L is variable. In this case, the maximum power is transferred when the load resistance is equal to source resistance. If $R_L = R_S$ and $X_S = -X_L$ then,

$$Z_L = R_L + jX_L$$

$$= R_S - jX_S = Z_S^*$$

This means that the maximum power transfer occurs when the load impedance is equal to the complex conjugate of the source impedance Z_S .

Example 5 : For the circuit shown in Fig. 2.21, determine the value of load impedance for which source delivers maximum power. Calculate the value of the maximum power.

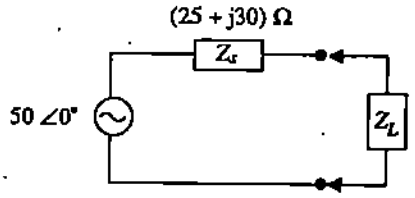


Fig. 2.21: Example 5.

Solution : As we know, the maximum power will be transferred to the load when load impedance is complex conjugate of the source impedance i.e.

$$Z_L = Z_S^* = 25 - j30$$

when $Z_L = 25 - j30$, the current passing through the circuit is

$$i(t) = \frac{50 \angle 0°}{25 + j30 + 25 - j30} = \frac{50 \angle 0}{50} = 1 \angle 0°$$

Maximum power delivered to the load is

$$P = I_0^2 R_L = (1)^2 \times 25 = 25 \text{ W}$$

SAQ 5

For the circuit shown in Fig. 2.22, the resistance R_S is variable from 2 Ω to 25 Ω. Determine what value of R_S results in maximum power transfer across the terminals *XY*.

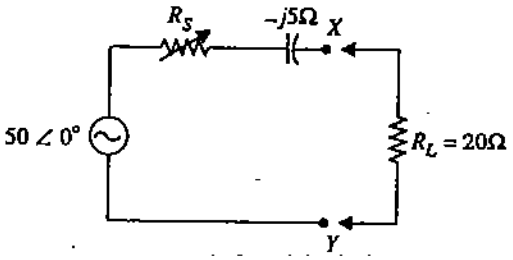


Fig. 2.22:

2.5 THEORY OF PASSIVE FILTERS

The wave filters were first invented by G.A. Campbell and O.J. Lobel of the Bell Telephone laboratories. A filter is essentially a reactive network that freely passes the desired bands of frequencies while almost totally suppressing all other bands. A filter is constructed from purely reactive elements, for otherwise the attenuation would never become zero in the pass band of the filter network. Filters differ from simple resonant circuits (discussed in section 2.3) in providing a substantially constant transmission over the band which they accept. Ideally, a filter should produce no attenuation in the desired band called the "pass band" and should provide infinite attenuation in all other frequencies called the "Stop band". The frequency which separates pass band and stop band is defined as the "Cut off frequency" (f_c). A filter may, in principle, have any number of pass bands separated by attenuation bands. However, they are classified into four common types : low

pass, high pass, band pass and band reject. In coming sections, we will discuss about these types of filters in detail. Before we get into these filters, we would like to study the equations of filter networks. The study of the behavior of any filter requires the calculation of its propagation constant (γ), attenuation(α), phase shift (β) and its characteristic impedance (Z_0).

T-Network

Consider a symmetrical T-network as shown in Fig. 2.23. As we know, if the image impedance at port 11' and port 22' are equal to each other, the image impedance is then called "Characteristic" or "iterative impedance" (Z_0). Thus, if the network shown in Fig. 2.23 is terminated in Z_0, its input impedance will also be Z_0. Clearly, the input impedance for this network will be :

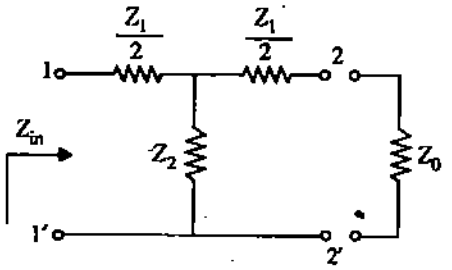


Fig. 2.23: Symmetrical T-network.

$$Z_{in} = \frac{Z_1}{2} + Z_2 \| \left(\frac{Z_1}{2} + Z_0\right)$$

$$= \frac{Z_1}{2} + \frac{Z_2\left(\frac{Z_1}{2} + Z_0\right)}{\frac{Z_1}{2} + Z_2 + Z_0}$$

Also, $Z_{in} = Z_0$

$$\therefore \quad Z_0 = \frac{Z_1}{2} + \frac{2Z_2\left(\frac{Z_1}{2} + Z_0\right)}{\frac{Z_1}{2} + Z_2 + Z_0}$$

$$= \frac{Z_1^2 + 2Z_1Z_2 + 2Z_1Z_0 + 2Z_1Z_2 + 4Z_0Z_2}{2(Z_1 + 2Z_2 + 2Z_0)}$$

$$4Z_0^2 = Z_1^2 + 4Z_1Z_2$$

$$Z_0^2 = \frac{Z_1^2}{4} + Z_1Z_2$$

The characteristic impedance of a symmetrical T-network is,

$$Z_0 = \sqrt{\frac{Z_1^2}{4} + Z_1Z_2}$$

The characteristic impedance can be expressed in terms of the open circuit impedance Z_{OC} and short circuit impedance Z_{SC} of the T-network.

Clearly, $Z_{SC} = \frac{Z_1}{2} + \frac{\frac{Z_1}{2} \times Z_2}{\frac{Z_1}{2} + Z_2} = \frac{Z_1^2 + 4Z_1Z_2}{2Z_1 + 4Z_2}$

and $$Z_{OC} = \frac{Z_1}{2} + Z_2$$

$$Z_0^2 = Z_{OC} \times Z_{SC} = Z_1 Z_2 + \frac{Z_1^2}{4}$$

$$\rightarrow Z_0 = \sqrt{Z_{OC} Z_{SC}}$$

By definition, the propagation constanst (γ) of the T-network is given by (See Fig. 2.24)

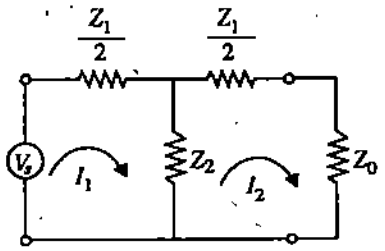


Fig. 2.24: Definition of propagation constant.

$$\gamma = \log_e \frac{I_1}{I_2}$$

Taking the mesh equation, we get

$$I_1 Z_2 = I_2 \left(\frac{Z_1}{2} + Z_2 + Z_0 \right)$$

$$\rightarrow \quad \frac{I_1}{I_2} = \frac{\frac{Z_1}{2} + Z_2 + Z_0}{Z_2} = e^{\gamma}$$

$$\rightarrow \quad Z_0 = Z_2 (e^{\gamma} - 1) - \frac{Z_1}{2}$$

The characteristic impedance of T-network is

$$Z_0 = \sqrt{\frac{Z_1^2}{4} + Z_1 Z_2}$$

Putting this in above equation and simplifying, we obtain :

$$(e^{\gamma} - 1)^2 = \frac{Z_1 e^{\gamma}}{Z_2}$$

$$\rightarrow \quad e^{2\gamma} + 1 - 2e^{\gamma} = \frac{Z_1}{Z_2 e^{-\gamma}}$$

$$\rightarrow \quad e^{\gamma} + e^{-\gamma} - 2 = \frac{Z_1}{Z_2}$$

Dividing both side by 2, we get

$$\frac{e^{\gamma} + e^{-\gamma}}{2} = 1 + \frac{Z_1}{2 Z_2}$$

$$\cosh \gamma = 1 + \frac{Z_1}{2 Z_2}$$

Also $$\sinh \gamma = \sqrt{\cosh^2 \gamma - 1}$$

$$= \frac{1}{Z_2}\sqrt{Z_1 Z_2 + \frac{Z_1^2}{4}} = \frac{Z_0}{Z_2}$$

$$\tanh\gamma = \frac{Z_0}{Z_0 + \frac{Z_1}{2}}$$

π-network

Consider a symmetrical π-section shown in Fig. 2.25. When the network is terminated in Z_0 at port 22', its input impedance is given by :

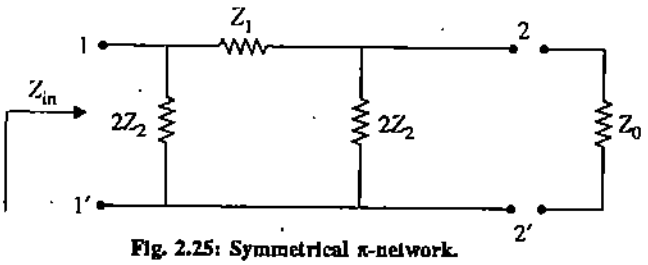


Fig. 2.25: Symmetrical π-network.

$$Z_{in} = \frac{2Z_2\left[Z_1 + \frac{2Z_2 Z_0}{2Z_2 + Z_0}\right]}{Z_1 + \frac{2Z_2 Z_0}{2Z_2 + Z_0} + 2Z_2}$$

By definition of characterstic impedance, $Z_{in} = Z_0$

$$\therefore \quad Z_0 = \frac{2Z_2\left[Z_1 + \frac{2Z_2 Z_0}{2Z_2 + Z_0}\right]}{Z_1 + \frac{2Z_2 Z_0}{2Z_2 + Z_0} + 2Z_0}$$

$$\rightarrow \quad Z_0^2 = \frac{4Z_1 Z_2^2}{Z_1 + 4Z_2}$$

$$\rightarrow \quad Z_0 = \sqrt{\frac{Z_1 Z_2}{1 + \frac{Z_1}{4Z_2}}}$$

The propagation constant of a symmetrical π- network is same as that for a symmetrical T-network and is given by

$$\cosh\gamma = 1 + \frac{Z_1}{2Z_2}$$

2.5.1 Constant-*K* Low Pass Filter

By definition, a low pass (LP) filter is one which passes without attenuation all frequencies upto the cut off frequency (f_c) and attenuates all other frequencies greater then f_c. This attenuation characteristic of an ideal LP filter is shown in Fig. 2.26. A network, either T or π, is said to be of the constant *K*-type if Z_1 and Z_2 of the network satisfy the relation :

$$Z_1 Z_2 = K^2$$

where Z_1 and Z_2 are impedance in the T and π section as shown in Fig. 2.27 (a) and

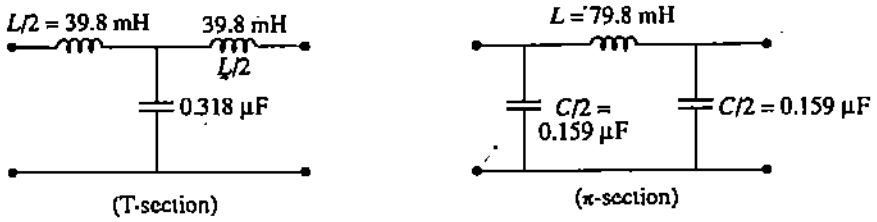


Fig. 2.29: T and π section of low pass filter (Answer to Example 6)

2.5.2 Constant *K*-High Pass Filter

By definition, a high pass (HP) filter attenuates all frequencies below a designated cut off frequency f_c, and pass frequencies above f_c. Thus, the pass band of this

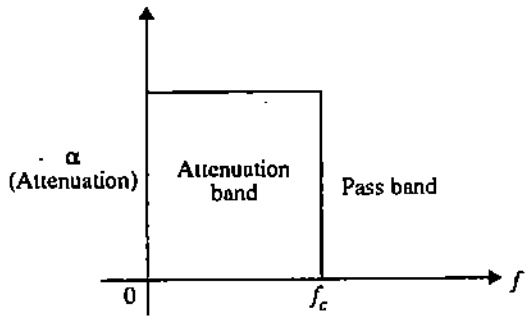


Fig. 2.30: Ideal characteristic of a HP Filter.

filter is the frequency range above f_c and stop band is the frequency range below f_c. The attenuation characteristic of an ideal HP filter is shown in Fig. 2.30. Constant *K*-high pass filter can be obtained by changing the position of series and shunt arms of the network shown in previous section. The prototype high pass filters are shown in Fig. 2.31 (a) and (b) where $Z_1 = \frac{1}{j\omega C}$ and $Z_2 = j\omega L$.

$$Z_1 Z_2 = \frac{L}{C} = K^2$$

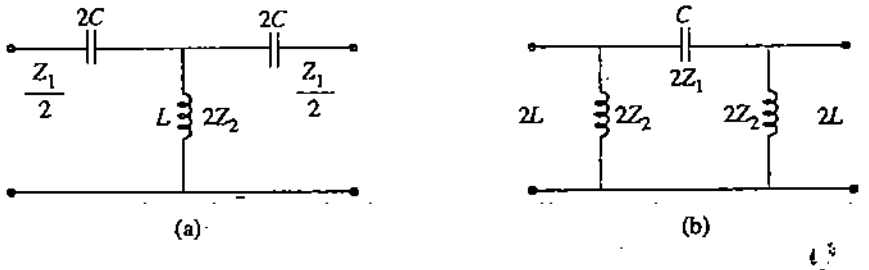


Fig. 2.31: Constant *K*-type HP filter (a) T section (b) π section.

$$\therefore \quad K = \sqrt{\frac{L}{C}}$$

The cut off frequencies are given by $Z_1 = 0$ and $Z_1 = -4Z_2$.

$$Z_1 = 0 \Rightarrow \frac{1}{j\omega C} = 0 \Rightarrow \omega \to \infty$$

$$Z_1 = -4Z_2$$

$$\Rightarrow \frac{-j}{\omega C} = -4j\omega L$$

$$\Rightarrow f_c = \frac{1}{4\pi\sqrt{LC}}$$

The variation of reactances (Z_1 and Z_2) with frequency are shown in Fig. 2.32. As

seen from the figure, the filter transmits all frequencies between $f = f_c$ and $f = \infty$. The point f_c from the graph is a point at which $Z = -4Z_2$. We know,

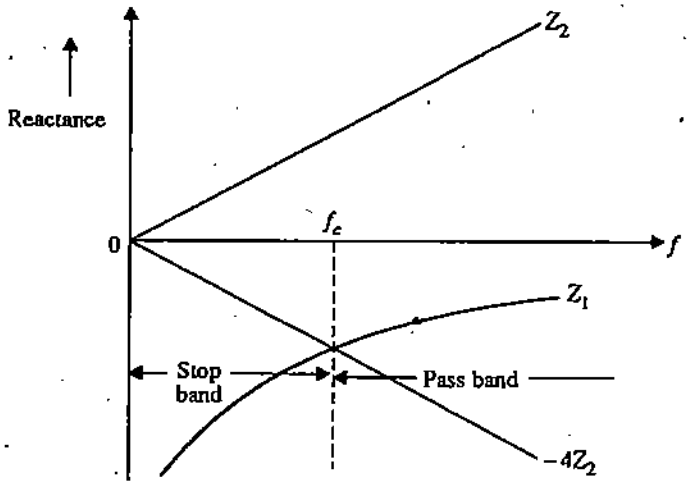


Fig. 2.32: Variation of reactances with frequency.

$$\sinh\frac{\gamma}{2} = \sqrt{\frac{Z_1}{4Z_2}} = \sqrt{\frac{-1}{4\omega_0^2 LC}}$$

Also, $$f_c = \frac{1}{4\pi\sqrt{LC}}$$

$\therefore$ $$\sinh\frac{\gamma}{2} = j\frac{f_c}{f}$$

In the pass band, $-1 < \frac{Z_1}{4Z_2} < 0$, $\alpha = 0$ or the region in which $\frac{f_c}{f} < 1$ is a pass band

with β = phase shift $= 2\sin^{-1}\left(\frac{f_c}{f}\right)$.

In the attenuation band, $\frac{Z_1}{4Z_2} < -1 \Rightarrow \frac{f_c}{f} > 1$

Here, $\alpha = 2\cosh^{-1}\left[\frac{Z_1}{4Z_2}\right] = 2\cosh^{-1}\frac{f_c}{f}$

and $\beta = -\pi$

Example 7 : Design a high pass filter having a cut off frequency of 1 KHz with a load resistance of 600 ohm.

Solution : Here, $f_c = 100\,\text{Hz}$ and $K = 600\,\Omega$

$$L = \frac{K}{4\pi f_c} = \frac{600}{4 \times \pi \times 1000} = 47.74\,\text{mH}$$

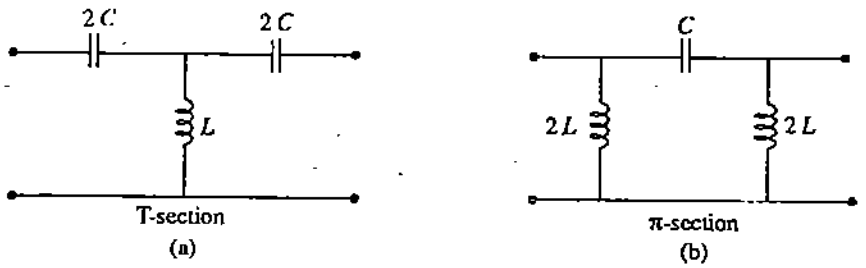


Fig. 2.33:

$$C = \frac{1}{4\pi K f_c} = 0.133\,\mu F$$

T and π sections are shown in Fig. 2.33.

2.5.3 Band Pass filter

By definition, a band pass filter is one which passes frequencies between two designated cut off frequencies and attenuates all other frequencies. Fig. 2.34 shows an ideal attenuation characteristic of a band pass filter. A band pass filter may be obtained by using a low pass filter followed by a high pass filter in which the cut off frequency of the LP filter is above the cut off frequency of HP filter, the

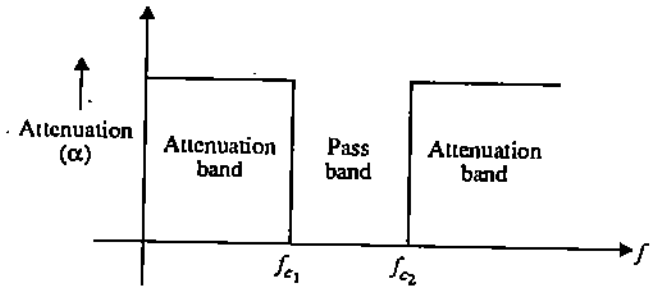


Fig. 2.34: Ideal attenuation characteristic of a band pass filter.

overlap thus allowing only a band of frequencies to pass. This is not economical in practice, it is more economical to combine the low and high pass functions into a single filter section.

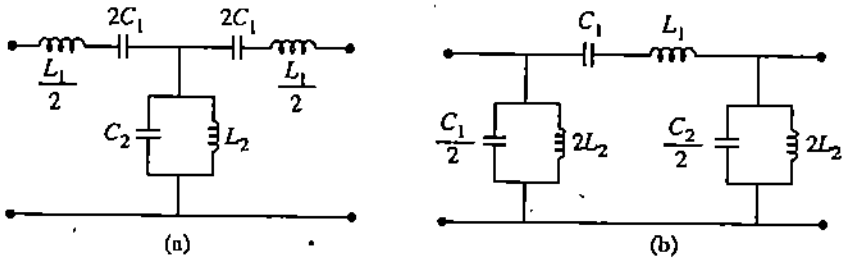


Fig. 2.35: Band pass filter.

Consider, the circuit shown in Fig. 2.35 (a) and (b), each arm has a resonant circuit with same resonant frequency i.e., the resonant frequency of the series arm and the resonant frequency of the shunt arm are made equal to obtain band pass characteristics.

Clearly, for condition of equal resonant frequencies

$$L_1 C_1 = L_2 C_2$$

$$Z_1 = \text{Impedance of series arm} = j\left(\frac{\omega^2 L_1 C_1 - 1}{\omega C_1}\right)$$

$$Z_2 = \text{Impedance of shunt arm} = \left(\frac{j\omega L_2}{1-\omega^2 L_2 C_2}\right)$$

$$\therefore \quad Z_1 Z_2 = \frac{-L_2}{C_1}\left(\frac{\omega^2 L_1 C_1 - 1}{1 - \omega^2 L_2 C_2}\right)$$

As, $L_1 C_1 = L_2 C_2$

$$\therefore \quad Z_1 Z_2 = \frac{L_2}{C_1} = \frac{L_1}{C_2} = K^2$$

where K is a constant. Thus the filter is a constant K-type.

Pass band : $-1 < \frac{Z_1}{4Z_2} < 0$ and at cut off frequency

$$Z_1 = -4Z_2$$

$$\rightarrow \quad Z_1^2 = -4Z_1 Z_2 = -4K^2$$

$$\rightarrow \quad Z_1 = \pm j2K$$

i.e., the value of Z_1 at lower cut off frequency is equal to the negative of the Z_1 at upper cut off frequency.

It can be shown, f_0 = resonant frequency = $\sqrt{f_1 f_2}$

SAQ 6

Determine cut off frequency for the LP filter shown in Fig. 2.36 (a) and (b).

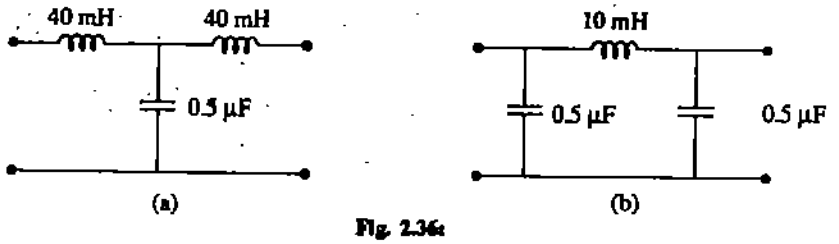


Fig. 2.36

SAQ 7

Determine the cut off frequency for the HP filter shown Fig 2.37 (a) and (b).

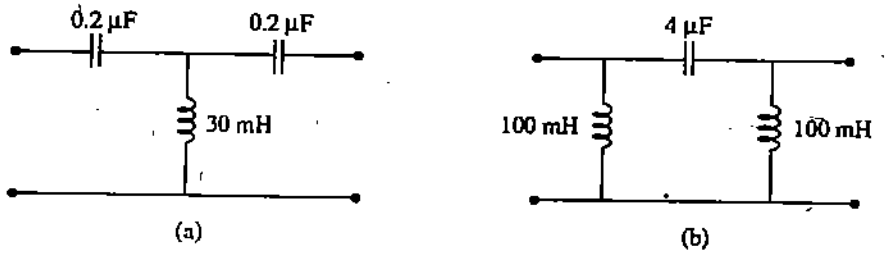


Fig. 2.37

2.6 ATTENUATORS

An attenuator is a two port resistive network and is used to reduce the signal level by a given amount. In number of application, it is necessary to introduce a specified loss between source and a matched load without altering the impedance relationship. Attenuators may be symmetrical or asymmetrical, and can be either fixed or variable. A fixed attenuator of constant attenuation is called a "Pad". Variable attenuators are used as volume controls in radio broadcasting, speed control of fans etc. Attenuators are also used in laboratory to obtain a small value of voltage or current for testing circuits. Attenuation is generally expressed in decibels (dB) or in nepers. Attenuation offered by a network in dB is given as follows:

$$\text{Attenuation in dB} = 10 \log_{10}\left(\frac{P_1}{P_2}\right)$$

Where P_1 is input power and P_2 is output power.

$$R_2 = R_0 \coth\left(\frac{\alpha}{2}\right)$$

$$R_1 = R_0 \left[\frac{e^{\alpha} - e^{-\alpha}}{2}\right]$$

By definition of propagation constant , we get

$$e^{\gamma} = \frac{I_1}{I_2} = N$$

Here, $\gamma = \alpha \rightarrow e^{\alpha} = N$

using this, we get

$$R_1 = R_0\left[\frac{N - 1/N}{2}\right] = \frac{R_0 (N^2 - 1)}{2N}$$

Also, $$R_2 = R_0 \coth\left(\frac{\alpha}{2}\right) = R_0 \frac{\cosh\left(\frac{\alpha}{2}\right)}{\sinh\left(\frac{\alpha}{2}\right)}$$

$$= R_0 \frac{e^{\alpha/2} + e^{-\alpha/2}}{e^{\alpha/2} - e^{-\alpha/2}}$$

$$= R_0 \frac{e^{\alpha} + 1}{e^{\alpha} - 1} = R_0 \frac{(N+1)}{(N-1)}$$

The expressions for R_1 and R_2 are called the design equations of the symmetrical π-attenuator.

Example 9 : Design a π-type attenuator to give 40 dB attenuation and to have a characteristic impedance of 100 Ω.

Solution : We know,

$$N = \text{antilog}\left(\frac{\text{dB}}{20}\right)$$

$$= \text{antilog}\left(\frac{40}{20}\right)$$

$$= 100$$

$$\therefore \quad R_1 = \frac{R_0 (N^2 - 1)}{2N} = 100 \frac{9999}{2 \times 100}$$

$$= 5000\,\Omega$$

$$R_2 = R_0 \frac{N+1}{N-1} = 100 \times \frac{101}{99}$$

$$= 102\,\Omega$$

2.6.3 Lattice Attenuator

A symmetrical resistance lattice is shown in Fig. 2.40 (a). The series and the diagonal arms of the network can be specified in terms of the characteristic impedance Z_0 and propagation constant, γ. We know that the characteristic impedance of symmetrical network is geometric mean of the open and short circuit impedance of the network.

The circuit of Fig. 2.40 (a) is redrawn in Fig. 2.40 (b) to calculate open and short circuit impedances.

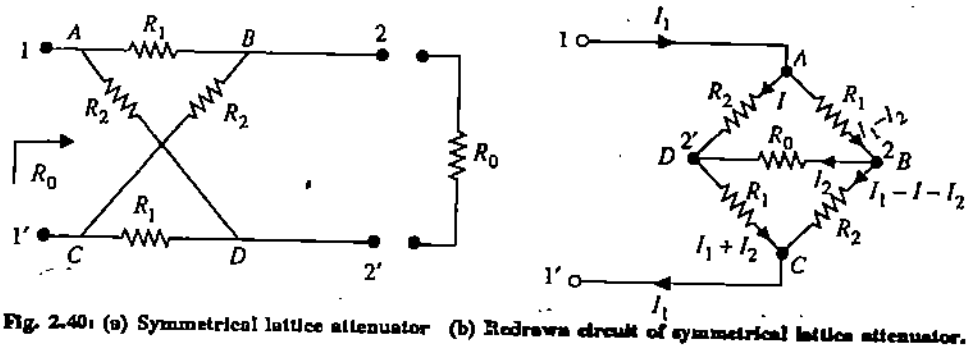


Fig. 2.40: (a) Symmetrical lattice attenuator (b) Redrawn circuit of symmetrical lattice attenuator.

$$Z_{SC} = \frac{2R_1R_2}{R_1 + R_2}$$

$$Z_{OC} = \frac{R_1 + R_2}{2}$$

Hence, $$Z_0 = R_0 = \sqrt{Z_{OC}Z_{SC}} = \sqrt{\frac{R_1 + R_2}{2} \times \frac{2R_1R_2}{R_1 + R_2}}$$

$$= \sqrt{R_1R_2}$$

In Fig. 2.40 (b), applying kirchoff's laws, we get

$$V_1 = I_1R_0 = (I_1 - I)R_1 + I_2R_0 + (I + I_2)R_1$$

$$I_1R_0 = R_1(I_1 + I_2) + I_2R_0$$

$$I_1(R_0 - R_1) = I_2(R_1 + R_0)$$

$$\therefore \quad \frac{I_1}{I_2} = \frac{R_1 + R_0}{R_0 - R_1} = \frac{1 + R_1/R_0}{1 - R_1/R_0}$$

$$N = e^{\alpha} = \frac{I_1}{I_2} = \left[1 + \frac{R_1}{R_0}\right] \Big/ \left(1 - \frac{R_1}{R_0}\right)$$

$$\therefore \quad e^{\alpha} = \frac{1 + \sqrt{R_1/R_2}}{1 - \sqrt{\frac{R_1}{R_2}}} \quad \left[\text{putting } R_0 = \sqrt{R_1/R_2}\right]$$

$\rightarrow$ α = Propagation Constt.

$$= \log_e\left[\frac{1 + \sqrt{R_1/R_2}}{1 - \sqrt{R_1/R_2}}\right]$$

Also, from $N = \dfrac{1 + \dfrac{R_1}{R_0}}{1 - \dfrac{R_1}{R_0}}$

$\rightarrow$ $$R_1 = R_0\left(\frac{N - 1}{N + 1}\right)$$

also, $$R_2 = R_0\left(\frac{N + 1}{N - 1}\right)$$

The above equations are called design equations for lattice attenuator.

Example 10: Design a symmetrical lattice attenuator to have characteristic impedance of 100Ω and attenuation of 20 dB.

Solution: Given $R_0 = 100\,\Omega$ and attenuation = 20 dB

We know, $N = \text{antilog}\left(\frac{\text{dB}}{20}\right) \Rightarrow \text{antilog}\left(\frac{20}{20}\right) = 10$

From design equations for symmetrical lattice network

$$R_1 = R_0\left(\frac{N-1}{N+1}\right) = 100 \times \frac{10-1}{10+1} = \frac{900}{11} = 82.54\,\Omega$$

$$R_2 = R_0\left(\frac{N+1}{N-1}\right) = 100 \times \frac{10-1}{10+1} = \frac{900}{11} = 82.54\,\Omega$$

$$= 100 \times \frac{11}{9} = \frac{1100}{9} = 122.22\,\Omega$$

The resulting lattice attenuator is shown in Fig. 2.41.

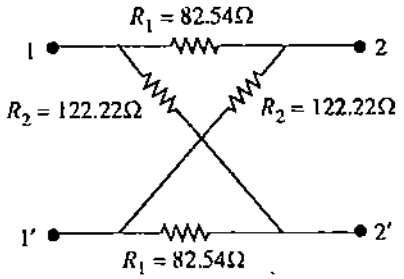


Fig. 2.41:

SAQ 8

Design a T-type attenuator to give an attenuation of 20 dB and to work in a line of 800 Ω

SAQ 9

Design a π-type attenuator to give an attenuation of 20 dB and to have characteristic impedance of 500 Ω.

SAQ 10

Design a symmetrical lattice type attenuator to give attenuation of 100 dB and to have characteristic impedance of 1000 Ω.

2.7 SUMMARY

- The frequency at which the resonance occurs is called resonant frequency.
- At resonant frequency the capacitive reactance and inductive reactance satisfy the following relation, $X_L = X_C$
- Band width of *RLC* series circuit is $\frac{R}{2\pi L}$
- For series resonant circuit quality factor (or figure of Merit) is given by $Q = \frac{X_L}{R}$.
- For parallel circuit, Q-factor is given by $Q = \omega_0 RC$.
- Maximum power transfer occurs when the load impedance is equal to the complex conjugate of the source impedance.

- Filter can be classified as : Low pass, High pass and Band pass filters.
- An attenuator is a network which is used to reduce the signal level by a given amount.
- Attenuation offered by a network in dB is given by

$$\text{Attenuation in dB} = 10 \log \frac{P_1}{P_2}$$

Where P_1 is input power and P_2 is output power.

2.8 TERMINAL QUESTIONS

1. A signal generator supplies a 30V, 100 Hz signal to a series circuit shown in Fig. 2.42. Determine the impedance, the line current and phase angle of the given circuit.

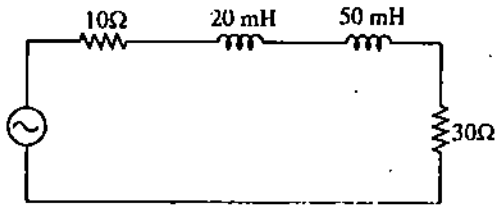


Fig. 2.42

2. For the circuit shown in Fig. 2.43, determine the value of R_c for which the circuit resonates.

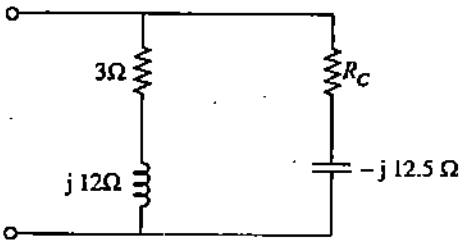


Fig. 2.43

3. Deduce

(i) $(Z_0)_{T\text{-network}} = \sqrt{\frac{Z_1^2}{4} + Z_1 Z_2}$

(ii) $(Z_0)_{\pi\text{-network}} = \sqrt{\frac{Z_1 Z_2}{1 + \frac{Z_1}{4Z_2}}}$

(iii) $\sinh \frac{\gamma}{2} = \sqrt{\frac{Z_1}{4Z_2}}$

2.9 SOLUTIONS AND ANSWERS

1. $V_S = \sqrt{V_R^2 + V_L^2} = \sqrt{(70)^2 + (20)^2} = 72.8 \text{ V}$

Phase angle $\theta = \tan^{-1}\left(\frac{V_L}{V_R}\right)$

$$= \tan^{-1}\left(\frac{20}{70}\right) \approx 15.95^\circ$$

2. $V_s = \sqrt{V_R^2 + V_C^2} = \sqrt{(20^2) + (30^2)} = 36\text{ V}$, Phase angle $(\theta) = \tan^{-1}\left(\frac{V_C}{V_R}\right) = \tan^{-1}\left(\frac{30}{20}\right) \approx 56{\cdot}3^\circ$

3. $Q = \frac{\omega_0 L}{R}$

$$5 = \frac{2\pi \times 500 \times 0.1}{R}$$

$$\rightarrow \quad R = 4\pi\Omega$$

$$\omega_0^2 = \frac{1}{LC}$$

$$C = \frac{1}{L \times \omega_0^2} = \frac{1}{0.1 \times 4\pi^2 \times 500^2}$$

$$= \frac{1}{100000 \times \pi^2} = 10^{-7}\text{ F} = 0.1\,\mu\text{F}$$

4. $f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.2 \times 10 \times 10^{-6}}} = 112.5\text{ Hz}$

$$Q = \frac{\omega L}{R} = 2.83$$

$$f_1 = f_0 - \frac{R}{4\pi L} = 92.6\text{ Hz}$$

$$f_2 = f_0 + \frac{R}{4\pi L} = 132.39\text{ Hz}$$

BW = Band width $= f_2 - f_1 = 39.79\text{ Hz}$

5. In the circuit shown, the resistance R_L is fixed. Hence the maximum power transfer theorem does not apply. Maximum current flows the circuit when R_S is minimum. For, the maximum current,

$$R_S = 2\ \Omega$$

Total impedance of circuit $Z = R_S - j5 + R_L$

$$= 2 - j5 + 20 = 22 - j5$$

$$= \sqrt{(22^2) + (5^2)}\, e^{j\tan\left(\frac{-5}{22}\right)}$$

$$= 22.56 \angle -12.8^\circ$$

$$\therefore \qquad I(t) = \frac{50 \angle 0^\circ}{22.56 \angle -12.8^\circ} = 2.22 \angle 12.8^\circ$$

Maximum power $= (2.22)^2 \times 20 = 98.6\text{ W}$

6. (a) T - network : $\frac{L}{2} = 40\text{ mH}, C = 0.5\,\mu\text{F}$

$$K = \sqrt{\frac{L^2}{C}} = 400\ \Omega$$

$$f_c = \frac{K}{L\pi} = 1591\text{ Hz} = \frac{1}{\pi KC}$$

(b) π - network $\frac{C}{2} = 0.5\,\mu F : L = 10\,mH$

$$K = \sqrt{\frac{L}{C}} = 100\,\Omega$$

$$f_c = \frac{K}{L\pi} = \frac{1}{\pi KC} = 3183\,Hz$$

7. (a) T-network : $2C = 0.2\ \mu F$

$\Rightarrow C = 0.1\ \mu F,\ L = 30\ mH$

$$f_c = \frac{1}{4\pi\sqrt{LC}} = \frac{K}{4\pi L}$$

$$= \frac{1}{4\pi\sqrt{0.1 \times 30 \times 10^{-3}}}$$

(b) π - network $2L = 100\ mH \Rightarrow L = 50\ mH$

$C = 4\ \mu F$

$$K = \sqrt{\frac{L}{C}} = \sqrt{\frac{50 \times 10^{-3}}{4 \times 10^{-6}}}$$

$$f_c = \frac{1}{4\pi KC}$$

8. $N = \text{antilog}\left(\frac{dB}{20}\right)$

$= \text{antilog}\left(\frac{20}{20}\right) = 10$

$$R_1 = R_0\frac{(N-1)}{(N+1)} = \frac{800 \times 9}{11} = \frac{7200}{11}\,\Omega$$

$$R_2 = \frac{2NR_0}{N^2-1} = \frac{2 \times 10 \times 800}{99} = \frac{16000}{99}\,\Omega$$

9. $N = \text{antilog}\left(\frac{20}{20}\right) = 10$

$$R_1 = \frac{R_0(N^2-1)}{2N} = \frac{500 \times 99}{2 \times 10}$$

$= 2475\,\Omega$

$$R_2 = \frac{R_0(N+1)}{(N-1)} = 500 \times \frac{11}{9} = \frac{5500}{9}\,\Omega$$

10. $N = \text{antilog}\left(\frac{100}{20}\right) = 10^5$

$$R_1 = \frac{R_0(N-1)}{N+1} = 10^3 \times \frac{10^5-1}{10^5+1} = 10^3\,\Omega$$

$$R_2 = \frac{R_0(N+1)}{N-1} = 10^3 \times \frac{10^5+1}{10^5-1} = 10^3\,\Omega$$

TQs

1. $Z_{Total} = 40 + j\,43.98$

semiconductors (elemental, compound or oxides) whose conductivity can easily be manoeuvred to suit the requirement. In this unit we will confine ourselves to elemental semiconductors & their basic properties in order to understand the physics of semiconductor devices. The most important are the electrical properties and their modification by doping. This can be understood from their energy band structure. A detailed explanation of the energy bands is a part of solid state physics course, however, the main features will be given in coming sections. Since most of the semiconductor devices likes diodes, transistors, field effect transistor (FET) and metal oxide semiconductor field effect transistors (MOSFET) are made of either Silicon or Germanium, it will be important to know some parameters of Silicon and Germanium, which are listed below in Table 3.1

Table 3.1

Parameters	Silicon (Si)	Germanium (Ge)
Atomic Number	14	32
Atomic Weight	28.08	72.60
Density ($Kg\,m^{-3}$)	2.33×10^3	5.33×10^3
Melting point (°C)	1420	937
Atoms per unit volume (m^{-3})	5×10^{28}	4.42×10^{28}
Relative permmittivity (ϵ_r)	11.8	16
Atomic diameter (nm)	0.235	0.246
Energy band gap Eg (ev)	1.12	0.66

In coming sections you will read application of these semiconducting material in fabricating $p-n$ junction diodes and their use as rectifier, detector, voltage reference; junction transistor, their characteristics, biasing and configuration in which it can be used as an amplifier; field effect transistor and MOSFET. We will start this unit with introduction to vacuum tubes for historical reasons. Although the use of vacuum tubes is very limited now as it has been completely replaced by semiconductor devices, yet they find some applications in ultra high frequency amplifying devices and high power (MW) electronic applications. The details of amplifier circuit, oscillator circuit and power supplies, will be dealt in BLOCK-2 of this course.

Objectives

After going through this unit you will be able to

- describe thermionic emission and concept of space charge limited operation and functioning of vacuum diode, triode, tetrode and pentode,
- explain the fundamentals of semiconducting material and their energy band diagram for intrinsic as well as extrinsic case,
- explain basic mechanism for transport of charge carriers in semiconductors,
- draw voltage-current characteristics of bulk semiconductor, $p-n$ junction diode and zener diode,
- describe functioning of bipolar junction transistor (BJT), field effect transistor (FET) and MOSFET.
- differentiate between basic features of devices like BJT, FET and MOSFET.

3.2 VACUUM TUBES

The thermionic vacuum diode, invented in 1903, was the first in chain of electronic devices that dominated the field of electronics till the invention of the transistor in

1948. The use of vacuum devices is now restricted to amplifying devices in ultra high frequency (MHz) and high power (MW) electronic applications.

3.2.1 Thermionic Emission

Electronic emission is the process by which the free electrons escape from the surface of metal. A metal is made up of atoms bound in crystal lattices, of electrons bound to the atoms, and of free electrons that are not bound to any particular locations in the metal. The free electrons are always in motion and travel more or less freely throughout the body of the metal. A certain minimum amount of energy must be given to the free electrons to enable it to escape from the metal. This amount of energy required at absolute zero temperature is known as "Work function" of the metal. It is expressed in electron-volts (eV). In thermionic emission, the electrons are emitted when a metal is supplied with heat energy. Suitable metals with low work functions values are tungsten in high-voltage (KV) tubes, thoriated tungsten in high power (KW) tubes and oxide coated metals in low-power electron tubes.

3.2.2 Vacuum Diode

The simplest form of a thermionic vacuum tube is the diode, consisting of a cathode heated by a filament and an anode enclosed in a evacuated glass or metal envelope (The pressure inside the chamber is roughly 10^{-6} mm of Hg or less). The

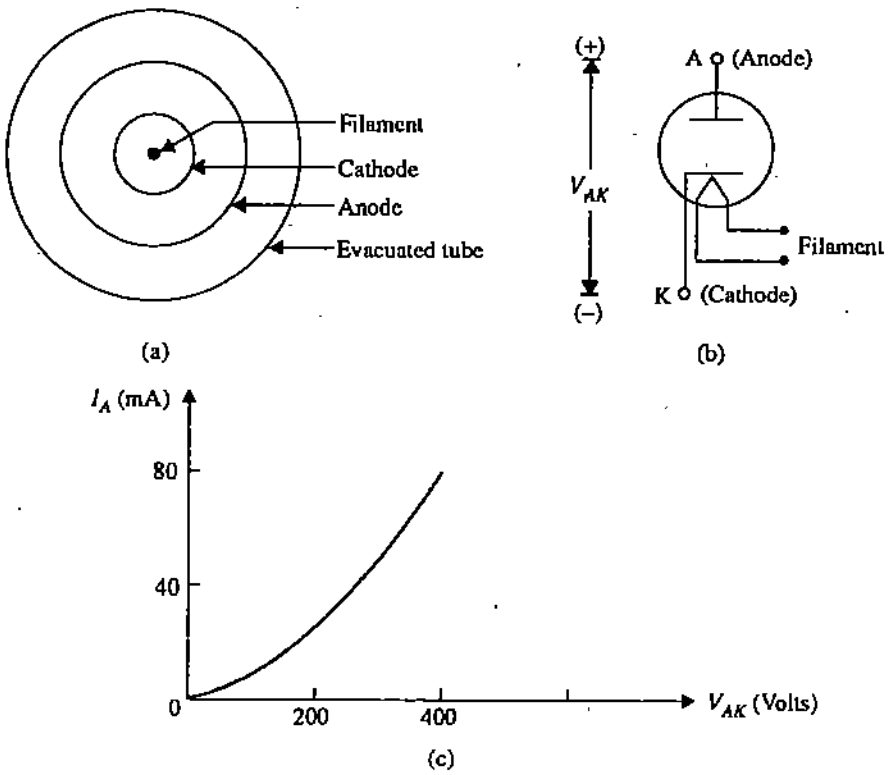


Fig. 3.1: A vacuum diode (a) construction (b) symbol and (c) volt-ampere characteristics.

construction and the symbol of a vacuum diode is shown in Fig. 3.1 (a) and (b) respectively. The volt-ampere characteristics of this device is shown in Fig. 3.1 (c).

When anode is maintained at a positive potential with respect to cathode, then the electrons emitted by the directly or indirectly heated cathode, are attracted by the anode and thus allows flow of current through diode. The volt-ampere characteristic clearly shows that this device conducts only in one direction i.e. when anode is positive with respect to cathode. Anode current is zero for zero and negative values of V_{AK}, the voltage between anode and cathode. One of the major problems associated with this device is "space-charge limited operation". This can be

explained as follows. In all the thermionic vacuum tubes, the electron emission of the cathode is at a much higher rate than that at which the electrons are drawn away by the anode. The resulting cloud of electrons near cathodes, called the negative space-charge, makes the anode current dependent on the anode potential and independent of the rate of emission, which depends on the temperature of the cathode. This phenomena is called "space charge limited operation". Clearly, in order to draw large anode current, we will require high potential difference between anode and cathode.

3.2.3 Vacuum Triode

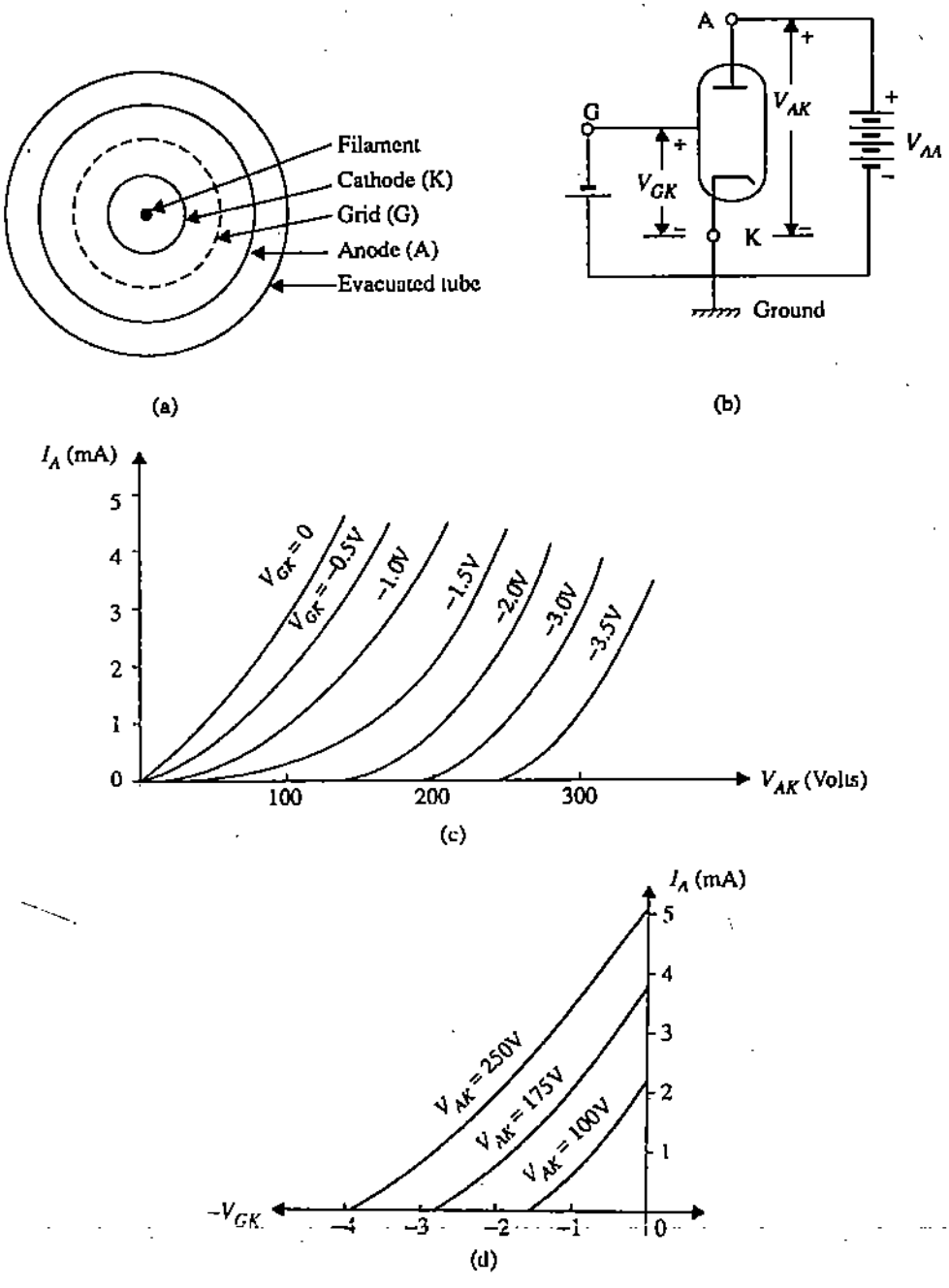


Fig. 3.2: A vacuum triode (a) construction (b) symbol along with dc biasing scheme (c) $V_{AK} - I_A$ and (d) $V_{GK} - I_A$ characteristics.

A vacuum triode has a third electrode, called "grid" due to its mesh like structure, introduced in the negative space-charge region nearer to the cathode as shown in Fig. 3.2 (a). The grid therefore has more effect than the anode in controlling the current flow between the anode and the cathode and hence it is called the "control grid".

The voltage drop between control grid (G) and cathode (K), V_{GK} is usually a few volts negative with respect to the cathode. The symbol of vacuum triode is shown in Fig. 3.2 (b). As control grid is nearer to the cathode, a much smaller voltage applied to the control grid can result in the same change of anode current as will be produced by a much larger voltage applied to the anode of the tube. This action of control grid also forms the basis of amplifying action of the triode.

In order to determine volt-ampere characteristics of a triode, we have to consider three variables namely V_{AK}, I_A and V_{GK}. The most commonly used plots are the anode characteristics ($I_A - V_{AK}$) with V_{GK} kept constant, and the transfer characteristics ($I_A - V_{GK}$) with V_{AK} kept constant as shown in Fig. 3.2 (c) and (d) respectively. The cut off grid voltage is that value of V_{GK} at which I_A becomes zero for a given value of V_{AK}.

The small signal parameters of triode can be determined by finding out dc operating point with the help of external voltage sources and resistors. In the near linear portion of the characteristics, their slope around a dc biasing point Q can be identified as follows :

Anode or plate resistance, $$r_p = \frac{\Delta V_{AK}}{\Delta I_A}\Bigg|_{V_{GK}=\text{Const.}}$$

Transconductance, $$g_m = \frac{\Delta I_A}{\Delta V_{GK}}\Bigg|_{V_{AK}=\text{Const.}}$$

Amplification factor, $$\mu = \frac{\Delta V_{AK}}{\Delta V_{GK}}\Bigg|_{I_A=\text{Const.}}$$

Clearly, $$\mu = r_p \times g_m \qquad (3.1)$$

Small Signal Models :

For small voltage and current variations around the Q-point, these small signal parameters can be considered to be constant and then a small change in I_A can be expressed as :

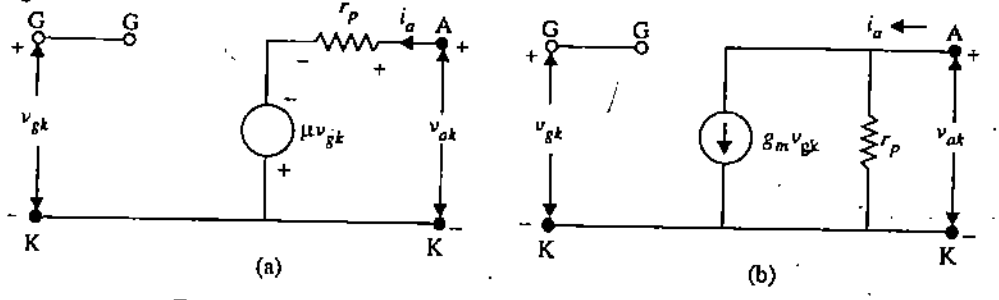


Fig. 3.3: Small signal models, (a) voltage source (b) current source.

$$I_A = f(V_{AK}, V_{GK})$$

$$\therefore \quad \Delta I_A = \frac{\partial I_A}{\partial V_{GK}}\Delta V_{GK} + \frac{\partial I_A}{\partial V_{AK}}\Delta V_{AK}$$

$$= g_m \Delta V_{GK} + \frac{I}{r_p}\Delta V_{AK}$$

$$\rightarrow \quad i_a = g_m v_{gk} + \frac{I}{r_p} v_{ak}$$

$$\rightarrow \quad v_{ak} = i_a r_p - g_m r_p v_{gk} = i_a r_p - \mu v_{gk} \qquad (3.2)$$

where i_a, v_{gk} and v_{ak} represent the varying components of currents, and voltages in the circuit. This equation can be replaced by circuit known as small signal model for triode, shown in Fig. 3.3 (a), and (b).

Figure 3.3 (b) can be understood by rewriting the above equation as :

$$\frac{v_{ak}}{r_p} = i_a - g_m v_{gk} \quad \left[\begin{array}{l}\text{Dividing both sides} \\ \text{by } r_p \text{ the equation} \\ v_{ak} = i_a r_p - g_m r_p v_{gk}\end{array}\right] \tag{3.3}$$

3.2.4 Vacuum Tetrode and Pentode

Vacuum Tetrode

The major problem associated with triode is its inter electrode capacitances. They are capacitance between grid and anode, grid and cathode, and anode and cathode. These capacitances become very effective at high frequencies resulting in instability in the action of Triode at such high frequencies. To overcome this limitation, a new electrode is introduced, giving us a four electrode tube called tetrode. The fourth electrode is called a "Screen grid". Structurally it is similar to control grid and is

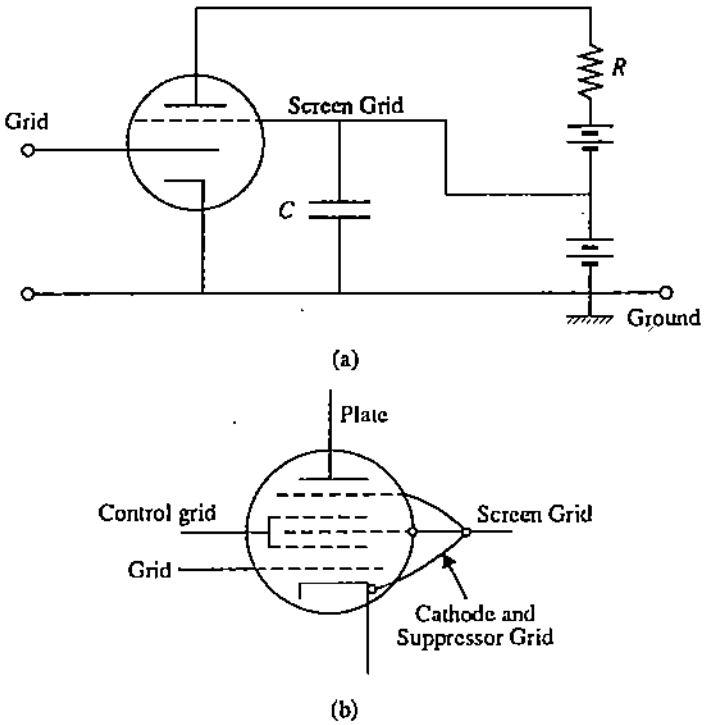


Fig. 3.41 (a) A tetrode with proper biasing (b) A Pentode.

placed between anode and control grid. It is operated at a fixed positive potential. The two main functions of the screen grid are (i) to increase the plate current by overcoming the space charge (ii) to reduce the capacitance between the control grid and the anode at high frequencies. A tetrode valve is shown in Fig. 3.4 (a).

Vacuum Pentode

The problem associated with tetrode is that when screen grid is at a higher potential than the anode, the primary electrons from the cathode accelerated by the screen grid hit the anode resulting in the emission of secondary electrons from the anode, which are attracted by the screen grid forming a screen current, which reduces the plate current. To avoid the decrease in plate current, a new electrode is inserted between the screen grid and the anode. It makes five electrode structure called Pentode. The new electrode is called the "Suppressor grid". It is kept at cathode potential. The purpose of suppressor grid is to return back the secondary electrons emitted by the anode thereby removing the dip in the plate current curve of tetrode. A Pentode valve is shown in Fig. 3.4 (b).

SAQ 1 Give examples of some elemental, compound and oxide semiconductors? How does the conductivity of oxide semiconductors change?

SAQ 2. Define "Work function" Explain thermionic emission.

SAQ 3. What do you understand by space charge limited operation? Explain this with reference to vacuum diode. How the adverse effect of space charge region controlled in a triode?

SAQ 4. Give volt-ampere characteristics of a vacuum triode and give the small signal parameters.

SAQ 5. What do you understand by small signal model of a triode. Give small signal model for a triode with a voltage source and a current source.

SAQ 6. Write notes on (i) Tetrode (ii) Pentode.

3.3. SEMICONDUCTOR MATERIALS

The term semiconductor denotes a solid-state material having a resistivity lying between that of a good insulator and of a metal i.e. lying in the range of 10^4 to 10^{-4} Ωm. Silicon, Germanium and Gallium Arsenide are the three most widely used semiconductors. Because of the predominance of silicon devices, we will confine our discussion to them. Semiconductor can be of two types : Intrinsic or Extrinsic. An intrinsic semiconductor is one which is pure and consists entirely of the same types of atoms in a perfect covalent tetrahedral crystalline structure. In order to obtain extrinsic or doped semiconductor minute, controlled quantities of trivalent (barium, gallium or indium) or pentavalent (phosphorous, arsenic or antimony) doping atoms are intentionally added to an intrinsic tertravalent semiconductor. Since impurity atom doping is very small, the basic crystal structure is unaltered. Most physical and chemical properties are essentially same and only the electrical properties change markedly.

3.3.1 Energy Band Diagram (Intrinsic Semiconductor)

A solid body consist of a host of atoms which strongly interact owing to small inter atomic distances. Instead of combination of discreate energy levels inherent in an individual atom, characteristic of a solid body is an aggregate of energy bands. Every band originates from a certain level which splits, as it were, as atoms come closer together. As a result, a crystal with an inter atomic spacing do features a definite arrangement of energy bands; the band diagram where (allowed) energy bands alternate with energy gaps, also called "forbidden bands" or "band gaps", is shown in Fig. 3.5(a)

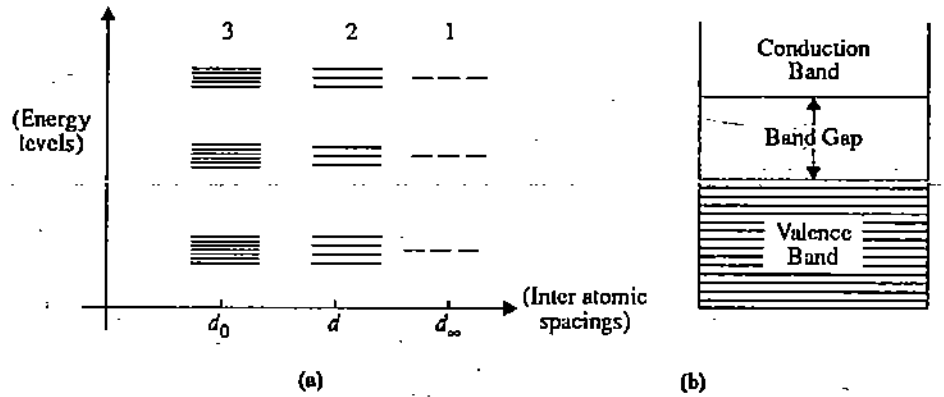


Fig. 3.5: Formation of energy bands (a) 1 → individual atomic levels ; 2 → aggregate of energy bands ; 3 → almost continuous energy bands (b) energy band diagram of intrinsic semiconductors at T=0K.

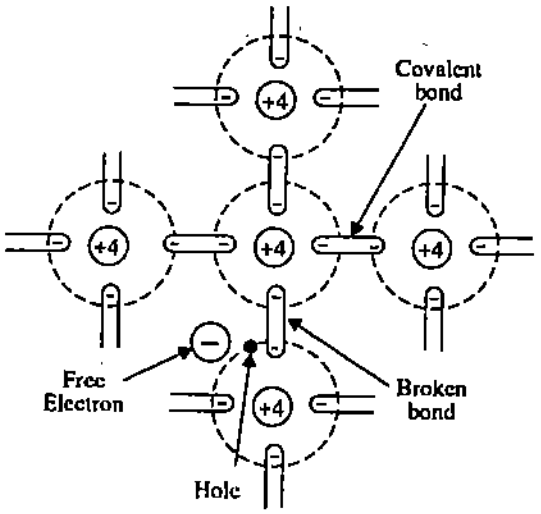


Fig. 3.6: Covalent bond model for intrinsic semiconductor with thermally generated electron-hole pair.

The upper energy band is a conduction band and the band below it is a valence band as shown in Fig. 3.5(b). At absolute zero, the valence band is always filled completely with electrons, whereas the conduction band is almost empty.

The silicon or geranium atoms are tetravalent as they have four valence electrons in their outermost orbit. A simplified model of tetravalent atoms consists of a core with a +4e charge surrounded by the four valence electrons. The arrangement is shown in Figure 3.6 in a simplified two dimensional form. Each of the four valence electrons of a particular atom is shared i.e. associated with each of the four nearest atoms forming strong covalent bonds. When a covalent bond is broken as shown in Fig. 3.6, the freed electron leaves behind a vacancy in the covalent bond. There is an excess of positive charge in the broken bond associated with this position of the missing electron. This vacant position or gap is called a "hole". Since breaking a covalent bond results in both a free electron and a hole, consequently, the hole concentration (p) and electron concentration (n) must be equal and

$$n = p = n_i \tag{3.4}$$

where n_i represents the intrinsic concentration of charge carriers. Thus the thermal agitation generates new electron-hole pairs. The electrons have a limited lifetime in the conduction band and periodically fall back to the valence band in a "recombination" process with energy of excitation appearing as heat energy. The lifetimes τ_n and τ_p of electrons and holes are very important parameters as they indicate the time required for the excess electrons and hole concentration to return to their equilibrium values. The intrinsic concentration n_i is very sensitive to temperature and is given by

$$n_i = A_0 T^{3/2} \exp\left(\frac{-qE_g}{2KT}\right) \tag{3.5}$$

where A_0 and E_g are material constants, K-Boltzmann Constant and T is temperature in K. The Term $\frac{KT}{q}$ appears very often in semiconductor physics and is generally denoted by symbol V_T (thermal voltage)

$$V_T = \frac{KT}{q} = \frac{T}{11.600} = 25\,\text{mV} \quad \text{at } T = 300\,\text{K}$$

clearly, both electrons and holes contribute to the conduction process in a semiconductor. However, the hole mobility μ_p is always less (≈ 3 times lower) than the electron mobillity μ_n due to the complexity involved in the motion of a hole.

The expression for conductivity (σ) can be given by

$$\sigma = q(n\mu_n + p\mu_p) \qquad (3.6)$$

In intririsic semiconductors $n = p = n_i$

3.3.2 Effect of Doping on Energy Band Diagram

As already explained in earlier sub-section, a doped semiconductor (may also be called extrinsic semiconductor) is one in which minute, controlled quantities of trivalent (for p-type semiconductor) or pentavalent (for n-type semiconductor) doping atoms are intentionally added to an intrinsic semiconductor (Si or Ge).

n-type semiconductor

Assume that a small amount of pentavalent element is added to the pure silicon. The resulting energy-band model and the two-dimensional bond structures are shown in Fig. 3.7 (a) and (b) respectively. The pentavalent doping atom is represented by an ion having $+5e$ charge surrounded by five valence electrons. Four of the five valence electrons of the impurity atom enter into convalent bonds with neighbouring tetravalent silicon atoms. The fifth electron is now loosely bound to the parent atom by an electrostatic force alone. In the presence of a small thermal energy (0.01 eV for Ge and 0.05 eV for Si) this extra electron becomes a free electron available for conduction even at low temperatures. The impurity atom is known as donor atom as it has donated one electron to the crystal. The donor atom occupies an energy level very near to the conduction band as shown in Fig. 3.7 (a). In the charge model, shown in Fig. 3.7 (c), only the immobile positively ionised impurity atoms along with the free charge carriers (electrons) which they have donated are shown. In Fig. 3.7 (c) the silicon atoms as well as the relatively small number of thermally generated electron-hole pairs are omitted for the sake of simplicity.

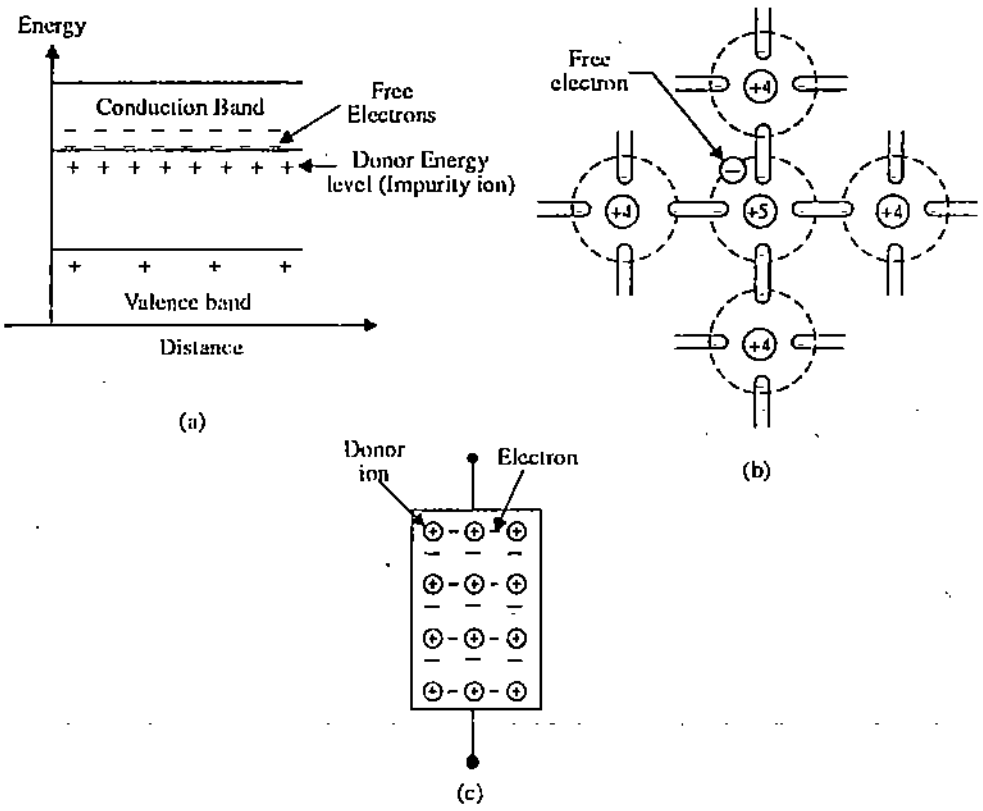


Fig. 3.7: Two dimension model for n-type semiconductors (a) energy-band (b) bond model (c) charge model.

p-type semiconductor

Assume that a small amount of trivalent element is added to the pure silicon. The

resulting energy-band model and the two dimensional bond structure are shown in Fig. 3.8 (a) and (b) respectively. The trivalent doping is represented by an ion having +3e charge surrounded by three valence electrons. These three valence electrons enter into covalent bonds with the neighbouring three tetravalent silicon atoms. A vacancy or hole exists in the fourth bond as shown in Fig. 3.8 (b). There is a possibility that a valence electron from a neighbouring atom hops into the vacancy. That is why doping atoms are called "acceptor impurity" as it accepts an electron. The negative acceptor ion occupy the energy level near the valence band as shown in Fig. 3.8 (a). The hole now can be assumed to be loosely bound to the parent impurity atom by electrostatic force alone which can be overcome easily by thermal excitation energy of 0.01 eV for Ge and 0.05 eV for silicon. Thus, even at low temperatures the impurity atom is ionised and the resulting hole is free to take part in conduction. In the charge model shown in Fig. 3.8 (c), only the immobile negatively ironised impurity atoms along with the hole are shown.

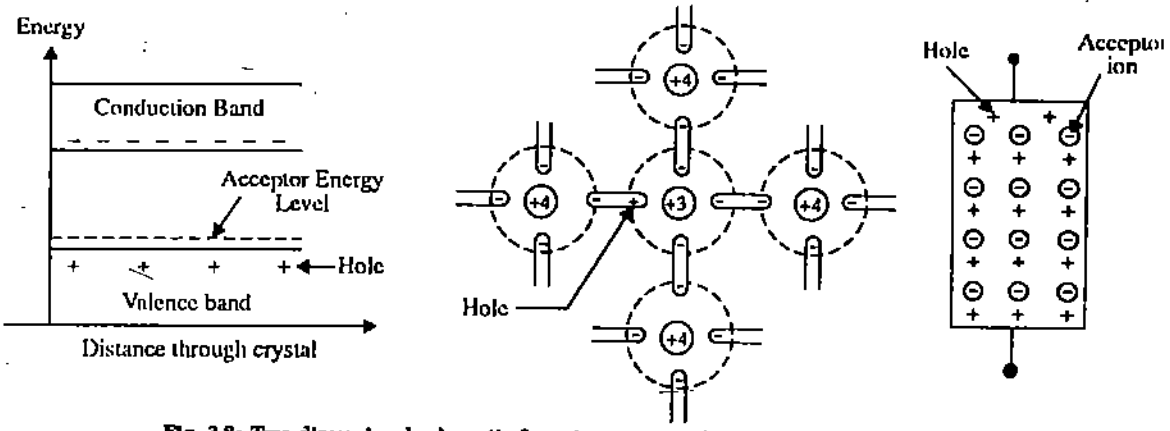


Fig. 3.8: Two dimensional schematic for *p*-type semiconductor (a) band structure (b) bond model (c) charge model.

Law of mass action

In the *n*-type (*p*-type) semiconductors, the number of holes (electrons) decrease below that, which would be available in the intrinsic semiconductor. This is because the rate of recombination increases due to the presence of a large number of free electrons (holes). Further, the law of mass-action states that under thermal equilibrium for any semiconductor, we have

$$np = n_i^2 \tag{3.7}$$

Thus the doping of intrinsic semiconductor enhances the number of majority carriers viz. electrons (holes) in *n*-type (*p*-type) semiconductor while suppressing the number of minority carries viz. holes (electrons) in the *n*-type (*p*-type) semiconductor. For conductivity of the doped semiconductors, the dominant majority carriers alone need to be considered.

Conductivity

(i) *n*-type semiconductors : $\sigma_n = q n_n \mu_n$ (3.8)

(ii) *p*-type semiconductors : $\sigma_p = q p_p \mu_p$ (3.9)

3.3.3 Transport of Charge Carriers in Semiconductors

In general, the charge carrier transport results from three processes, namely

(i) Temperature gradient

(ii) Drift due to the electric potential gradient

(iii) Diffusion due to the concentration gradient

Since most of the semiconductor devices are made to operate at constant temperature, therefore the charge transport due to temperature gradient is not

relevant for discussion here. We will just concentrate on the other two mechanisms for charge transport in semiconductors namely Drift and Diffusion.

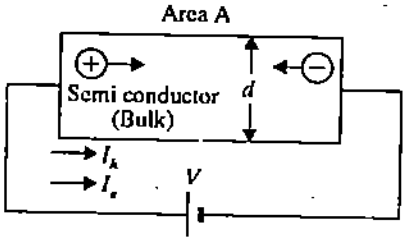


Fig. 3.9: Drift of charge carriers in semiconductor sample.

Drift of charge carriers under low fields

Suppose a voltage V is applied across a block of semiconductor of area A and thickness d as shown in Fig. 3.9. The electrons drift with velocity v_{de} and hole with v_{dh} in opposite directions. Since the hole carry a positive charge and electron negative charge, the current from both the carriers is in the same direction. Therefore current I can be expressed as :

$$I = \frac{V}{R} = q\,(nv_{de} + pv_{dh})\,A$$

J = current density $= \frac{I}{A} = q\,(nv_{de} + pv_{dh}) = \sigma E$

Where E is the electric field and σ, the electrical conductivity.

$$\sigma = q\left(\frac{nv_{de}}{E} + \frac{pv_{dh}}{E}\right) = q\,(n\,\mu_{de} + p\,\mu_{dh}) \qquad (3.10)$$

where μ_{de} and μ_{dh} are the drift mobilities of electron and hole. You may recall that mobility is defined as velocity per unit electric field.

High Field Conduction

The high field conduction can be divided into two regions :

(i) Saturation of drift velocity i.e. the current becomes independent of voltage (in turn electric field)

(ii) Breakdown, when current shows sudden increase with voltage.

Saturation of drift velocity

We know that in metals, the drift velocity (v_d) is always very much smaller than the thermal velocity of electrons $\left(v_{th} = \sqrt{\frac{3KT}{m_e}}\right)$: At room temperature ie, at 300 K, $v_{th} \approx 1 \times 10^7\ \text{cm s}^{-1}$ for free electrons. But in intrinsic semiconductors, which have high resistance and so it is possible to apply high electric field so that the drift velocity approaches the thermal velocity. When this situation reaches, the mobility becomes field dependent as additional scattering mechanisms come into play. The decrease in mobility with high electric field causes saturation of drift velocity. We can see for silicon, $\mu_e = 1500\,\text{cm}^2/\text{v-s}$, $v_d = 1 \times 10^7$ cm/s for electric field $E \approx 1 \times 10^4\ \text{V cm}^{-1}$. Typically, the current becomes independent of voltage once the electric field exceeds 10 KV/cm. The concept of saturation of drift velocity at high electric field is very important in understanding I-V characteristics of semiconductor devices .

Breakdown at very high electric fields

The drift velocity (v_d) being average velocity, individual electrons can have

velocities higher than average v_d. Hence, when the electric field in any semiconductor is increased above a certain value, some of the carriers gain enough energy so that they can excite electron-hole pairs by impact ionisation. These additional electron and holes generated by impact ionisation cause a sudden increase in the current, and the current shows a very rapid increase with voltage above the critical voltage for breakdown. A schematic representation of current density as a function of electric field is shown in Fig. 3.10. At low fields, we have ohmic region (OA), which changes into saturation region AB when drift velocity is saturated. The carrier concentration in OA and AB region is constant and the variation in current density is only due to variation in drift velocity with electric field. However, in region BC which is breakdown region, the sudden increase in current is due to the increase in number of carriers.

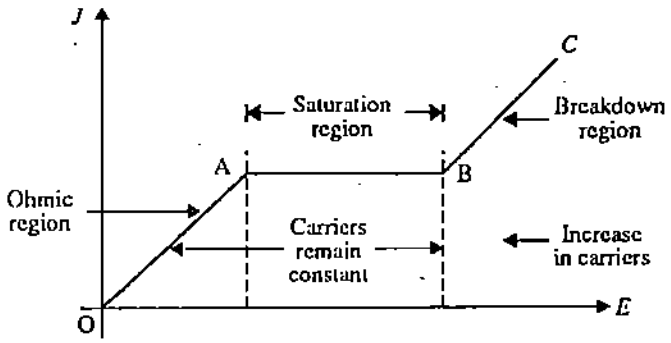


Fig. 3.10: Variation of current density as a function of electric field.

Diffusion of carriers due to concentration gradient

In diffusion mechanism, the transport of carriers is due to concentration gradient. When the concentration of charges at one place in a semiconductor is more than in other places, then the carriers from higher concentration region move to lower concentration region. This phenomena is not limited to the motion of electrons and holes but is a general phenomenon and we will see that it is used for doping impurities in semiconductor.

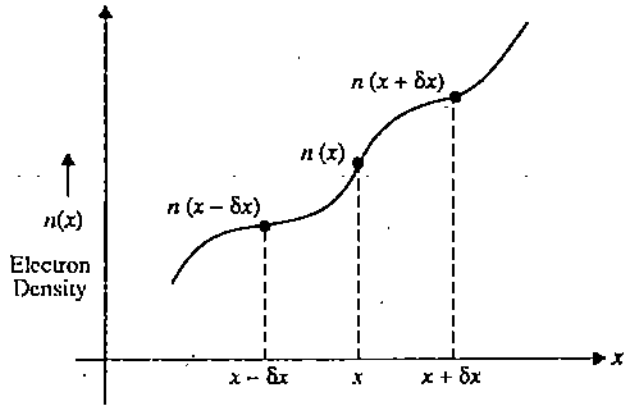


Fig. 3.11: Variation of electron density as a function of distance.

Let the variation of carrier concentration $n(x)$ as a function of distance x, be given by Fig. 3.11. We take δx as the mean free path (average distance covered by electrons before collision) and τ as the time between successive collision. The thermal velocity (v_{th}) can be written as :

$$v_{th} \simeq \frac{\delta x}{\tau}$$

The average rate of flow of charge carriers per unit area crossing the plane at x from left to right, F_x , can be expressed as :

$$F_x = \frac{1}{2}\left[\frac{\{n(x-\delta x)+n(x)\}}{2}\right]v_{th}$$

The factor half is coming because half of the carriers will be moving to the right, and the average number of charge carriers is half of the density of carriers at x and $x-\delta x$.

Taylor expansion of $n(x-\delta x) = n(x) - \frac{\partial n}{\partial x}\delta x + \cdots$

Neglecting higher order terms and substituting in above expression, we obtain

$$F_x = \frac{1}{2}\left[\frac{n(x)}{2} - \frac{1}{2}\frac{\partial n}{\partial x}\delta x + \frac{n(x)}{2}\right]v_{th}$$

$$= \frac{1}{2}\left[n(x) - \frac{1}{2}\frac{\partial n}{\partial x}\delta x\right]v_{th}$$

Similarly, the charge carriers passing per unit area per unit time from right to left at the interface x as shown in Fig. 3.11, F_x' can be expressed as :

$$F_x' = \frac{1}{2}\left[n(x) + \frac{1}{2}\frac{\partial n}{\partial x}\delta x\right]v_{th}$$

The net flow of charge carriers left to right per unit area per unit time can be obtained by taking difference of F_x and F_x' and can be given by :

$$F = F_x - F_x' = -\frac{1}{2}\delta x\, v_{th}\left(\frac{\partial n}{\partial x}\right)$$

The factor (1/2) in above equation arises from the simplifying assumptions. If we assume that average density between x and $x-\delta x$ is $n(x-\delta x)$ and between x and $x+\delta x$ as $n(x+\delta x)$, then the final expression will not have this factor of (1/2). Now, we define "diffusivity" or "diffusion constant" D ($cm^2 s^{-1}$) of charge carriers as

$$D = \frac{1}{2}\delta x\, v_{th} \simeq \delta x\, v_{th} \text{ (approx.)} \qquad (3.11)$$

Hence, the number of charge carriers moving from left to right per unit area per unit time can be expressed as :

$$F = -D\left(\frac{\partial n}{\partial x}\right) \qquad (3.12)$$

The current density $J = q\,F$,

where q is charge of the carrier, negative for electrons and positive for holes. For simple one dimensional case, the diffusion current due to the electrons and holes can be represented as

$$J_e(\text{diff.}) = q\,D_n\left(\frac{\partial n}{\partial x}\right) \qquad (3.13)$$

$$J_h(\text{diff.}) = -q\,D_h\left(\frac{\partial p}{\partial x}\right) \qquad (3.14)$$

The relation between the diffusion constant D and the mobility is called the Einstein's relation, and can be derived by assuming that the charge carriers behave like a free gas molecules. The Einstein's relation is given by

$$\frac{D}{\mu} = \frac{KT}{q} \qquad (3.15)$$

General case

In the general case when both concentration gradient and electric field E are present, the current carried by each type of carrier is given by

$$J_e = J_e(\text{drift}) + J_e(\text{diffusion}) \tag{3.16}$$

$$= q\mu_e nE + qD_e\left(\frac{\partial n}{\partial x}\right)$$

$$J_h = J_h(\text{drift}) + J_h(\text{diffusion}) \tag{3.17}$$

$$= q\mu_h pE - qD_h\left(\frac{\partial p}{\partial x}\right)$$

The total current density $J = J_e + J_h$ (3.18)

SAQ 7. Explain the formation of energy bands in intrinsic and extrinsic semiconductors. What difference do you observe?

SAQ 8. What do you understand by Law of mass action?

SAQ 9. Explain the variation of intrinsic carrier concentration with temperature.

SAQ 10. Explain the process of transport of charge carriers in semiconductors.

SAQ 11. Explain the variation of current density with electric field when it is low, high and very high.

3.4 p-n JUNCTION DIODES

You have already learned in previous section that the current flow in an extrinsic semiconductor is due to two mechanisms, namely drift and diffusion. The drift motion of carriers is caused by a potential gradient while diffusion takes place due to the carrier concentration gradient. The drift current is proportional to the electric field strength and the carrier concentration, while the diffusion current is proportional to only concentration gradient. Diffusion is important transport mechanism for minority carriers as their concentration gradient is steep. Majority carriers mainly contribute to the drift current as their concentration is more. By its very nature, diffusion is a slower transport mechanism as compared with drift. Diffusion is controlled by the number of electrons/holes crossing the barrier, while in drift the number of electrons is fixed at a temperature and the current increases with increasing field till saturation.

If we take an n-type semiconductor sample and diffuse p-type impurities into it, a $p-n$ junction is formed as shown in Fig. 3.12 (a). Only majority carriers and

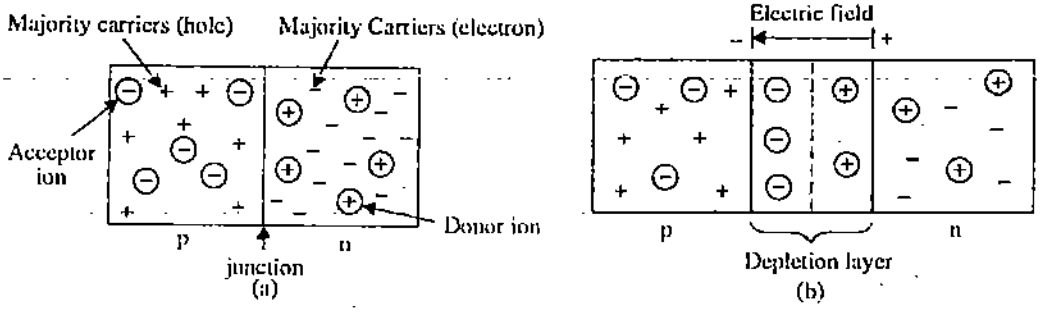


Fig. 3.12: Formation of p-n junction (a) carrier distribution (b) formation of charge depletion layer.

impurity ions are indicated on the *n*-and *p*-sides. Of course, on both *n* - and *p*-side, minority carriers also exists. When the junction is formed, because of the concentration gradient, holes from the *p*-side diffuse into the *n*-side and recombine with free electrons. Similarly, electrons from *n*-side diffuse to the *p*-side and recombine with holes. Such an exchange of mobile carriers occurs mainly in a narrow region around the junction. This region is called the "depletion layer" or "space-charge layer", as it becomes depleted of the free charge carriers, leaving behind the un neutralized immobile ions called space charge [due to positive ions on the *n*-side and negative ions in the *p*-side]. Such a space charge causes an electric field in the depletion region and a potential difference called the junction barrier potential develops across the *p-n* junction, making the *p*-side negative with respect to the *n*-side. This barrier potential cannot be measured with the help of a voltmeter. This potential barrier is of such a polarity that it opposes the diffusion of electrons from *n* to *p* region and holes from *p* to *n* region. However, the barrier helps the movement of minority carriers i.e., holes from the *n*-side can cross over to the *p*-side and electrons from *p*-side can cross over to the *n*-side. The magnitude of this minority carrier drift current is dependent only on the available number of minority carriers and is almost independent of the value of barrier potential. So, as the barrier potential builds up, the diffusion current goes on decreasing until the thermal equilibrium condition is reached i.e., when the drift current equals the diffusion current and the net current across the junction is zero. The barrier potential reaches the steady state value and does not increase any further as shown in Fig. 3.13 (a) and (b). It may be pointed out that the barrier potential for moderately doped Si *p-n* junction is of the order of 1 V and the barrier width of the order of 1μm, with the result that the electric field is of the order of 10^6 V cm^{-1} and the carrier passing through the junction barrier by drift current are already in the saturation state and so the drift current in *p-n* junction diode is indepehdent of voltage before we reach the break down.

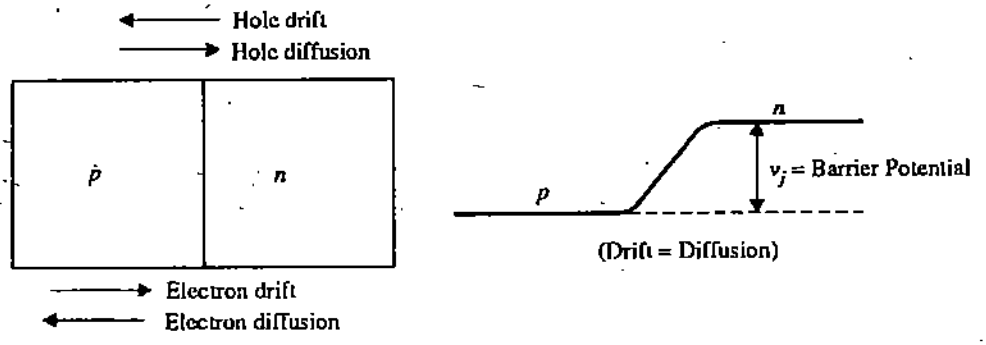


Fig. 3.13 (a) potential profile across the *p-n* junction (b) barrier potential.

As pointed out earlier, and external voltage from a battery at the junction can never exceed the barrier voltage because the barriers width cannot be made zero. In forward bias, the barrier width decreases as well as the barrier potential so the drift current is still under high field.

3.4.1 V-I Characteristics (p-n Junction with External Voltage)

Fig. 3.14 (a) shows a *p-n* junction with an external battery connected to it such that the positive terminal of the battery is connected to the *p*-side and the negative terminal to the *n*-side. Such a connection helps to reduce the barrier height as the external battery opposes the internal barrier potential. Hence, the diffusion current increases while minority carrier drift current is unaffected. A *p-n* junction connected in the above manner is said to be forward-biased as it conducts large amount of current in the forward direction which is taken as the direction of diffusion current flow. The junction presents a low impedance to the forward current flow.

On the other hand, if the battery polarity is reversed as shown in Fig. 3.14 (b), the

barrier height is increased. Hence majority carriers cannot diffuse. The minority carrier drift is unaffected. The *p-n* junction is said to be reversed biased and the minority-carrier drift current is called reverse saturation current. A reverse biased

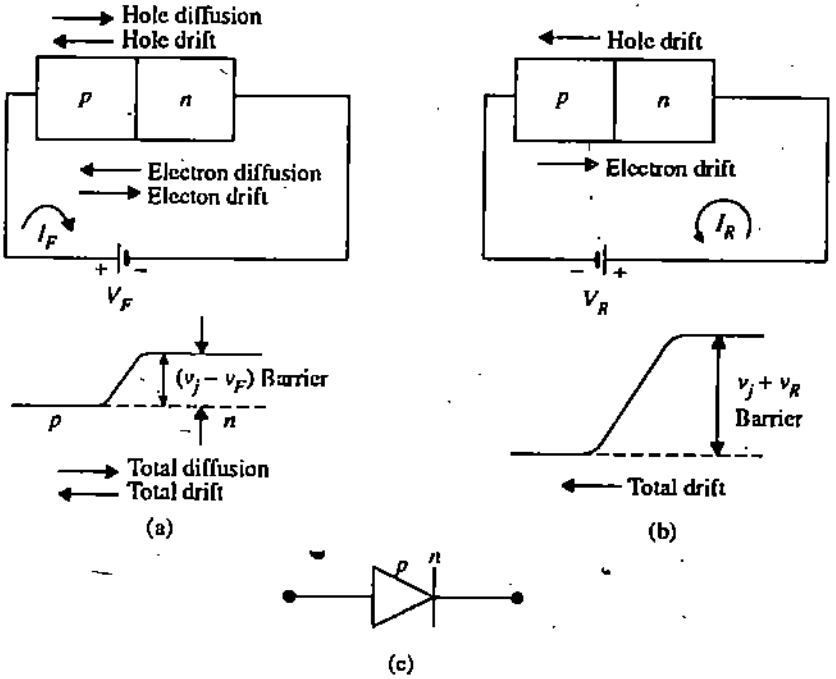


Fig. 3.14: (a) forward-biased *p-n* junction (b) reverse-biased *p-n* junction (c) symbol for *p-n* junction diode.

junction does not conduct much current in the reverse direction which is taken as the direction of minority carrier drift current .

In order to obtain current-voltage (*V-I*) characteristics of *p-n* junction diode we consider the followings.

(i) **Forward bias :** As we have already learned, the forward direction current is mainly due to diffusion current of majority carriers and is given by

$$I_F \ \alpha \ \exp \frac{qV}{KT}$$

$$\therefore \qquad I_F = I_S \exp \frac{qV}{KT} \qquad (3.19)$$

where I_S is reverse saturation current.

(ii) **Reverse bias :** Under reverse biased condition, it is the drift of minority

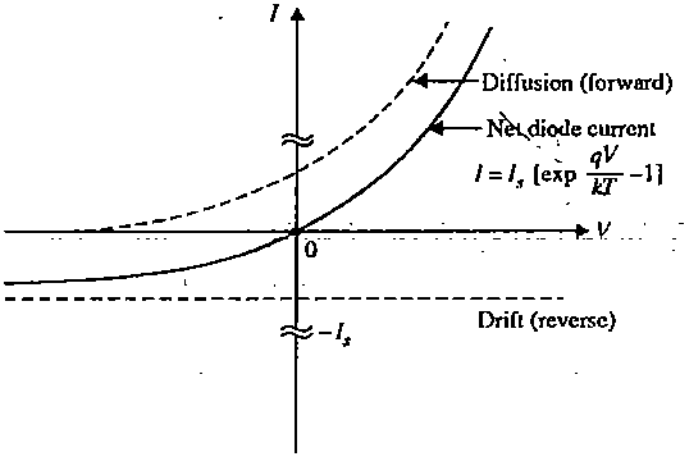


Fig. 3.15: *I-V* characteristics of a *p-n* junction diode.

carriers, which determine it. It is in opposite direction and has a constant value $-I_S$.

$$I_R = -I_S$$

Combining the two, the *I-V* characteristic equation is given by

$$I = I_S\left[\exp\frac{qV}{KT} - 1\right]$$

The characteristic is given in Fig. 3.15.

3.4.2 Applications (Rectifier, Detector and Reference Voltage)

In the application of devices, the major interest is in exploiting *V–I* characteristic for different applications without really worrying as to why such a characteristic has come, which has always been concern of physicist and has resulted into discovery of various new devices, while engineers have been able to exploit for day to day application of the devices. The specifications of the device is always supplied by the manufacturers. For example.

(a) IN 40001 is a *p-n* junction diode with $V_0 = 1.0\,V$ and $I_{max} = 1\,mA$.

(b) BC-108 is a *n-p-n* silicon transistor. The specifications are :
$I_{cmax} = 100\,mA$; $h_{FE} = 100 - 900$ at $I_{cmax} = 2\,mA$, $P_{tot}/MW = 360$,
$V_{CEO\,max}/V = 20$, $V_{EBO\,max}/V = 5$, $F_T/MHZ = 250$

(i) **Rectifiers :**

To start with we make an approximation, that the diode used in this circuit is ideal one i.e., it only conducts in forward direction and no conduction in reverse direction. Also, the forward impedance offered by the diode is taken as zero.

A rectifier circuit is one, which converts ac wave form to a unidirectional and pulsating one as shown in Fig. 3.16.

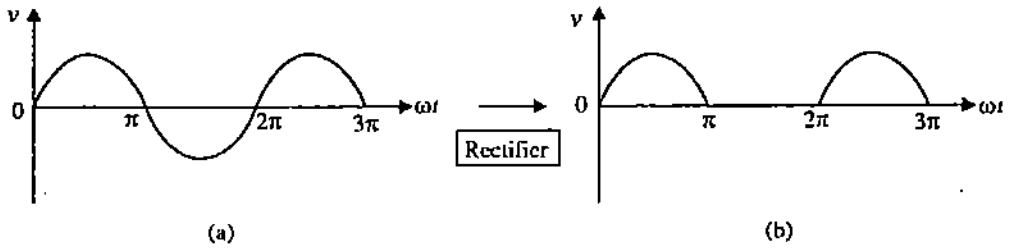


Fig. 3.16: Conversion of ac to unidirectional pulsating wave form.

A half wave rectifier circuit with resistive load is shown in Fig. 3.17. The voltage source is $V_S = V_m \sin \omega t$

Let R_s be the source resistance. When a supply of suitable voltage (as diode can withstand only few volts across it) is not available, a step down transformer can be used and V_s will be the secondary voltage of the transformer.

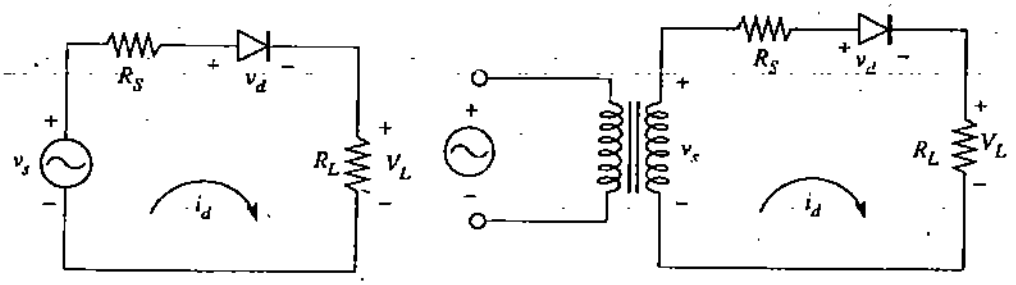


Fig. 3.17: Half wave rectifier circuit.

In the positive half cycle ($\theta \le \omega t \le \pi$) of V_s, it forward biases the given diode and produces a current in the positive direction. Clearly,

$$i_d = \frac{V_s}{R_s + R_L} = \frac{V_m \sin \omega t}{R_s + R_L} \text{ for } \theta \le \omega t \le \pi$$

$$= I_m \sin \omega t \text{ where } I_m = \frac{V_m}{(R_s + R_L)}$$

In the negative half cycle ($\pi \le \omega t \le 2\pi$), the diode gets reverse biased and no current flows in the circuit as diode will offer very high impedance i.e., it will behave as open circuit (infinite impedance). Hence

$$i_d = 0 \text{ for } \pi \le \omega t \le 2\pi$$

Also, $$V_L = i_d R_L = \frac{V_m R_L}{(R_s + R_L)} \sin \omega t \text{ for } 0 \le \omega t \le \pi$$

$$= 0 \text{ for } \pi \le \omega t \le 2\pi$$

Fig. 3.18 shows the load voltage wave form which is periodic containing rectified alternate half cycles.

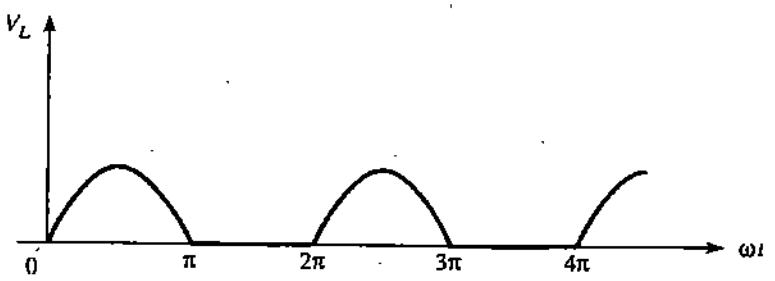


Fig. 3.18: Wave form of output voltage.

Since it is a periodic, finite and continuous wave form, it can be represented by a Fourier series given by

$$V_L = V_m \left[\frac{1}{\pi} + \frac{1}{2} \sin \omega t - \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{\cos 2k\omega t}{(2k+1)(2k-1)} \right]$$

It is clearly observed from above expression that the load voltage V_L consists of a dc component $\left(= \frac{V_m}{\pi} \right)$ and sinusoidal components at the fundamental frequency ω corresponding to the mains frequency and even harmonics of ω. Thus, the output contains frequencies which are not present in the input voltage. This is a consequence of the non linearity of the diode.

In order to have an assessment of the ac content of the output of a half wave rectifier circuit, the parameter that is used is known as "Ripple factor" and is defined as :

$$\text{Ripple factor } (\gamma) = \frac{\text{rms value of ac component of load voltage}}{\text{dc component of load voltage}}$$

If a signal consists of more than one frequency component the rms value of the total signal is related to the rms values of different frequency components by the following relation :

$$V_{rms} = \sqrt{V_{1rms}^2 + V_{2rms}^2 + \cdots}$$

where V_{1rms}, V_{2rms}... etc. are the rms values of each respective frequency component. In half wave rectifier, ac component consists of fundamental frequency and even harmonics.

$$V_{Lrms}^2 = (V_{Lacrms})^2 + (V_{Ldc})^2$$

$$\Rightarrow \quad (V_{Lacrms})^2 = (V_{Lrms})^2 - (V_{Ldc})^2$$

$$\therefore \quad \gamma = \text{Ripple factor} = \frac{(V_{Lacrms})}{(V_{Ldc})} = \sqrt{\frac{(V_{Lrms})^2 - (V_{Ldc})^2}{(V_{Ldc})^2}}$$

$$\therefore \quad \gamma = \sqrt{\left(\frac{V_{Lrms}}{V_{Ldc}}\right)^2 - 1} = \sqrt{\left(\frac{I_{Lrms}}{I_{Ldc}}\right)^2 - 1}$$

$$(I_{Lrms})_{\text{Halfwave}} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2 \omega t \, d(\omega t)}$$

$$= \frac{I_m}{2}$$

also, $I_{Ldc} = \frac{I_m}{\pi}$ [as $V_{Ldc} = \frac{V_m}{\pi}$, as seen from Fourier Expansion of load voltage]

$$\therefore \quad \gamma = \sqrt{\frac{\left(\frac{I_m}{2}\right)^2}{\left(\frac{I_m}{\pi}\right)^2} - 1} = \sqrt{\frac{\pi^2}{4} - 1} = 1.21$$

Form factor (F) : It is defined as the ratio of rms value of load voltage to the dc component.

$$\text{Form factor } (F) = \frac{V_{Lrms}}{V_{Ldc}} = \frac{I_{Lrms}}{I_{Ldc}}$$

$$= \frac{I_m/2}{I_m/\pi} = \frac{\pi}{2} = 1.57$$

Clearly, γ (Ripple factor) $= \sqrt{F^2 - 1}$

PIV : It's full form is peak inverse voltage. During negative half cycle, when $V_L = 0$ and diode acts as open circuit, the negative inverse voltage appears across the diode and the maximum inverse voltage is called "Peak Inverse Voltage" (PIV) $= V_m$. This is one of the important parameters for rectifiers.

Full wave rectifier : In the half wave rectifier, the output contains considerable ac content as compared with the dc content. This is because the rectified output contains only alternate half sinusoids. If we can rectify both the positive and negative half cycles of the input sine wave, then we can double the dc content and reduce the ac ripple. In order to realise this objective, we have to use two half wave

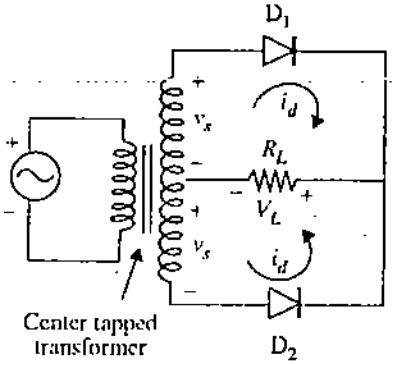


Fig. 3.19: Full wave rectifier circuit.

rectifiers connected to a common load, one rectifying the positive half cycle and the other negative half cycle. Such a full-wave rectifier circuit has to use two diodes which are fed by a center-tapped transformer as shown in Fig. 3.19.

In the positive half cycle ($\theta \le \omega t \le \pi$), diode D_1 conducts as it is forward biased and D_2 does not conduct as it is reverse biased. But during negative half cycle ($\pi \le \omega t \le 2\pi$) D_1 is open circuit as it is reverse biased and D_2 conducts, as it is forward biased. Both cycles, provide V_L i.e. voltage across load R_L with same polarity. The out put wave form is shown in Fig. 3.20.

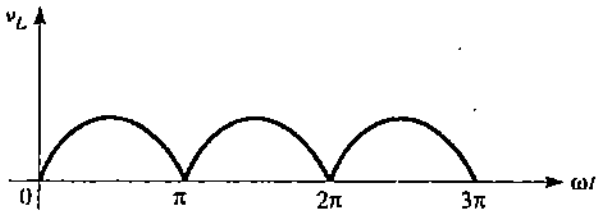


Fig. 3.20: Wave form of out put voltage in full wave rectifier.

The load voltage can be expanded in Fourier series given by

$$V_L = V_m \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{\cos 2k\omega t}{(2k+1)(2k-1)}\right]$$

Clearly, the load voltage contains dc component of $\frac{2V_m}{\pi}$, which is double of half wave rectifier and a set of sinusoidal components which are even multiple of fundamental frequency, ω,

Here, $V_{Ldc} = \frac{2V_m}{\pi} \Rightarrow I_{Ldc} = \frac{2I_m}{\pi}$

also, $V_{Lrms} = \frac{V_m}{\sqrt{2}}$ [since both cycles are involved]

$\Rightarrow$ $I_{Lrms} = \frac{I_m}{\sqrt{2}}$

Ripple factor $(\gamma) = \sqrt{\left(\frac{I_{Lrms}}{I_{Ldc}}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.482$

Form factor $(F) = \frac{I_{Lrms}}{I_{Ldc}} = \frac{\pi}{2\sqrt{2}} = 1.11$

$PIV = 2V_m$

Bridge Rectifier : In applications allowing floating output terminal i.e., no output terminal is grounded, a bridge rectifier can be used with advantage. The ripple factor and average diode current are the same as in the full-wave rectifier circuit.

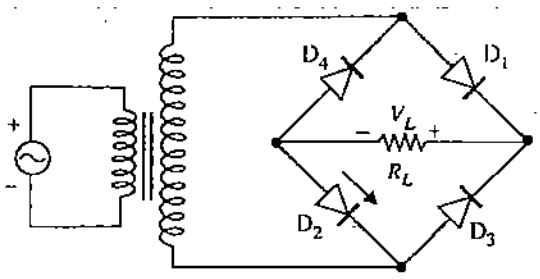


Fig. 3.21: Bridge rectifier circuit.

We also do not require center-tapped transformer as in the full wave rectifier circuit. The circuit for bridge rectifier is shown in Fig. 3.21.

In the positive half cycle ($\theta \le \omega t \le \pi$), diodes D_1 and D_2 are conducting as they are forward biased and D_3, D_4 are cut off. But in negative half cycle ($\pi \le \omega t \le 2\pi$), diodes D_4 and D_3 conduct as they are forward biased but D_1, D_2 are cut off as they are reverse biased. In both the cycles current flows in the same direction through load resistance R_L . Thus, the load will have a full wave rectified voltage. One major advantage of bridge rectifier circuit is that the PIV rating required of the diodes is half of the requirement for full-wave rectifier circuit.

So far, we have discussed rectifier circuit using ideal diode (Forward resistance = 0, reverse resistance = ∞). But in practical situations, we do not get such diodes. So with practical diodes, we can replace a forward biased diode by R_f and a reverse biased diode by R_r. You can also account for cut-in voltage (V_T) of the diode, by placing a battery of value V_T in series with forward biased diode so that it opposes the source.

(ii) Detector :

The peak detector circuit provides a dc output comparable to the peak value of the input voltage and therefore can be used as a dc power supply. The peak detector circuit is shown in Fig. 3.22. The operation of peak detector is understood by letting the input voltage $V_{in} = V_o \sin \omega t$ and assuming that load resistance is ∞. Then, during the first quarter-cycle, the diode conducts, and the capacitor will follow input and when $\omega t = \pi/2$, the capacitor will have charged to peak value V_0. When V_{in} decreases, the capacitor voltage cannot decrease because with $R_L = \infty$, the capacitor discharges through the diode in the reverse direction. Since diode does not conduct in reverse direction, so the capacitor cannot discharge. The load voltage therefore remains at the peak value V_o. But if load resistance is finite, then capacitor discharges with time constant R_LC, which is also shown in Fig. 3.22.

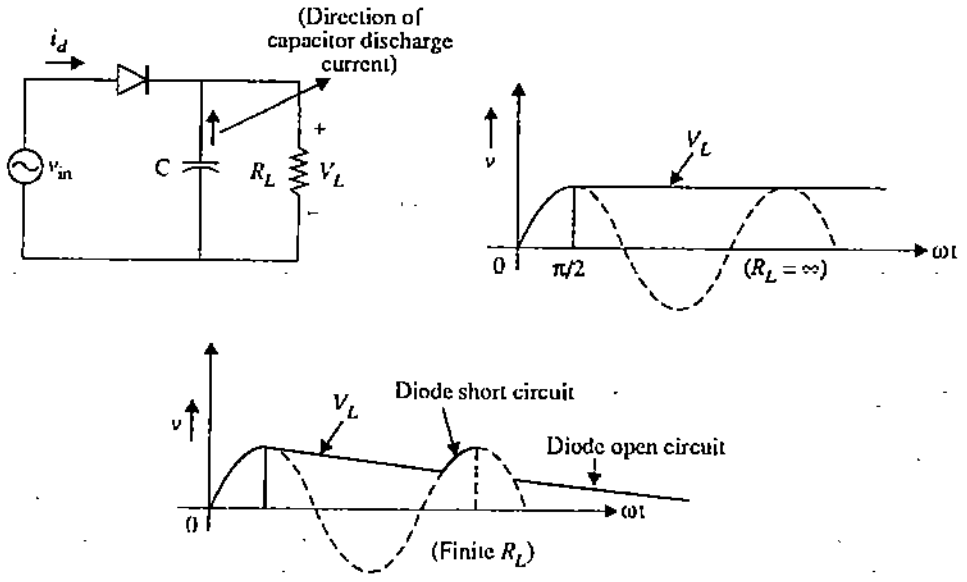


Fig. 3.22: The half wave peak detector.

(iii) Reference Voltage : (Zener diode)

As we have already learned in previous section that when diode is in reverse biased condition, then only a small reverse saturation current flows. It happens because the depletion layer width becomes wider and behaves like a dielectric. But if the p and n regions are heavily doped, the depletion layer of the p-n junction becomes very narrow and, the electric field strength in the depletion layer increases sufficiently to break covalent bonds and generate electron-hole pairs even in the reverse biased

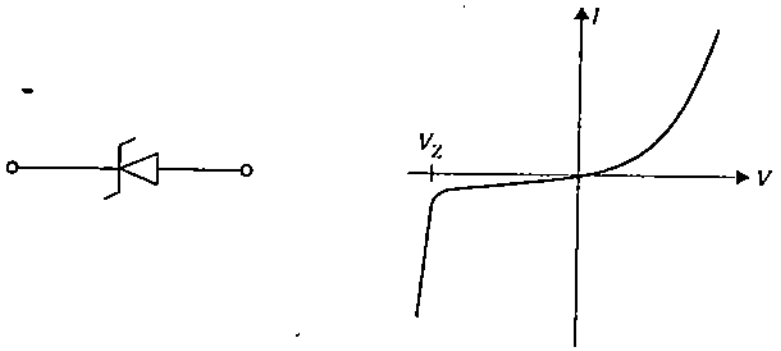


Fig. 3.23: Symbol and *V-I* Characteristic of Zener diode.

condition. Consequently, the reverse current rises abruptly. Such a phenomena is called "Zener break down" and the diode is called Zener diode. The symbol for the diode, its *V-I* characteristic is shown in Fig. 3.23.

As it is clear from the characteristics, in and around V_z, the current rises abruptly, suggesting that we can draw large current from zener diode at almost fixed voltage. This is property of a good voltage supply. Hence, a zener diode can be used as "reference voltage". A typical circuit is shown in Fig. 3.24.

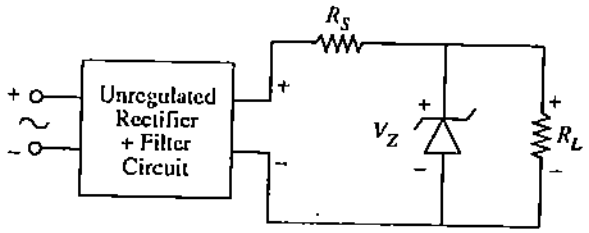


Fig. 3.24: Zener used as reference voltage.

SAQ 12 Explain transport of charge carriers in semiconductors.

SAQ 13. What do you understand by saturation of drift velocity?

SAQ 14. Explain the formation of barrier potential.

SAQ 15. Explain the *V-I* characteristics of the p-n junction diode.

SAQ 16. Define the terms : Ripple factor, Form factor and PIV.

SAQ 17. Explain the functioning of half wave rectifier and calculate value of ripple factor.

SAQ 18. Explain advantage of full wave rectifier over half wave rectifier. Calculate value of ripple factor.

SAQ 19. Compare full wave rectifier and bridge rectifier.

SAQ 20. Explain functioning of peak detector.

SAQ 21. Show how zener diode can be used as voltage reference.

3.5 TRANSISTORS

On the basis of the two terminal *p-n* properties described in section 3.4, an explanation of the physical operation of a three-terminal bipolar junction transistor (BJT) is developed in this section.

3.5.1 Action and Characteristics

A transistor is a single crystalline semiconducting material with three differently doped regions like the *n-p-n* or *p-n-p* structure. The three regions are called emitter, base and collector. Emitter is heavily doped and its role is to inject carriers into the base region. The base is lightly doped and is made very thin to reduce recombination losses in this region. The collector's doping level lies in between that of emitter and base. The schematic representation of *npn* and *pnp* transistors together with their circuit symbols are shown in Fig. 3.25 (a) and (b).

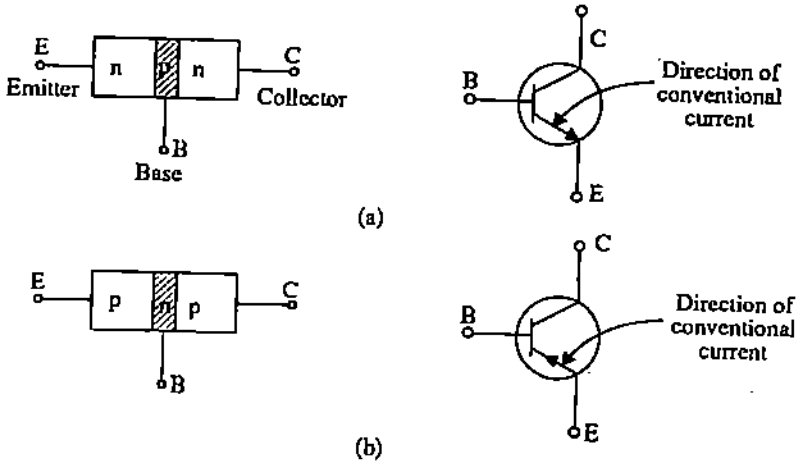


Fig. 3.25. (a) *npn* transistor & its circuit symbol (b) *pnp* transistor and its circuit symbol.

The transistor (*npn* or *pnp*) can be regarded as back to back connected diode. In order to understand transistor action, we forward bias the emitter-base junction and reverse bias the base-collector junction as shown in Fig. 3.26. (a) and (b).

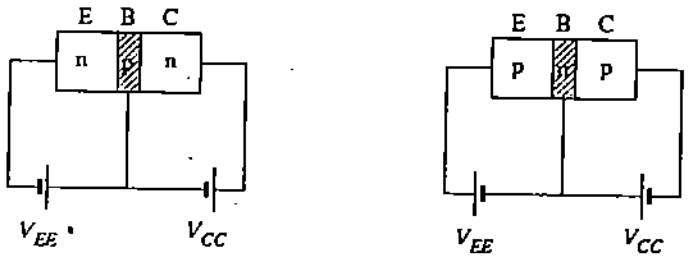


Fig. 3.26. (a) *npn* transistor with proper biasing (b) *pnp* transistor.

Let us consider forward biased emitter-base junction of *npn* transistor. The electrons from the emitter diffuse into the base and holes from base diffuse into the emitter. The base-collector junction is reverse biased. As the emitter base junction is forward biased, the electrons in the emitter and holes in the base move towards the junction. At this junction, some of the electrons recombine with holes and are lost. However, because of the extreme thinness of the base layer (typically less than 10^{-3} cm) and because of the attraction of the relatively high positive collector voltage, almost all the electrons diffuse through the base to the collector and produce an electron current in the collector. This current is called collector current (I_c) which is of the order of few milliamperes. To make the collection of electron efficient, the base-collector junction has a greater area than the emitter-base junction. Let us now consider the base current. This current is due to the small fraction of electrons which recombine in the thin base region. Since the base layer is very thin, the base current (I_B) is very small fraction of the collector's current (about 1%). In other words, about 99% of the electrons pass through the base without recombining with holes. Clearly, the basic current equation for any transistor is given by

$$I_E = I_B + I_C$$

Since $I_B << I_C$ so $I_E \simeq I_C$. In a typical transistors, I_E and I_C are a few milliamperes and I_B is a few micro amperes. The value of base current depends on base thickness,

bias voltages, doping levels of emitter, base, collector and the geometry of the transistor. The collector current I_C of a BJT is related to the forward base-emitter voltage V_{BE} by the relation:

$$I_C = I_{so}\, e^{V_{BE}/V_T}$$

Where I_{so} is a scale factor directly proportional to the cross sectional area of the emitter-base junction. If α_F is the factor of electrons reaching collector, and I_{CO} is the reverse saturation current in base-collector diode, then the collector current (I_C) can be written as :

$$I_C = \alpha_F\, I_E + I_{CO}$$

$$= \alpha_F\, (I_B + I_C) + I_{CO}$$

Here α_F is the dc current gain factor relating I_C & I_E [$\alpha \simeq 0.98$]

$$\Rightarrow \quad I_C = \left(\frac{\alpha_F}{1-\alpha_F}\right) I_B + \left(\frac{1}{1-\alpha_F}\right) I_{CO}$$

$$= \beta_F\, I_B + (\beta_F + 1)\, I_{CO}$$

Here, β_F is the dc current gain factor relating I_C & I_B

$$\beta_F = \frac{\alpha_F}{1-\alpha_F} = \frac{I_C - I_{CO}}{I_E - I_C + I_{CO}} = \frac{I_C - I_{CO}}{I_B + I_{CO}} \simeq \frac{I_C}{I_B}$$

The value of β ranges from 15 to 200. A small variation in α_F therefore causes large change in β_F . This results in BJT's of the same type number to have large variations in β_F . From above equation, we may obtain α_F in terms of β_F as :

$$\alpha_F = \frac{\beta_F}{\beta_F + 1}$$

V–I characteristics of BJT

A BJT is a three terminal device. Any one of these terminal can be used as the reference or common terminal for both the varying input v_i and output v_o signal. This gives rise to three possible configurations in which transistor can be used :

(i) common emitter configuration

(ii) common base configuration

(iii) common collector configuration

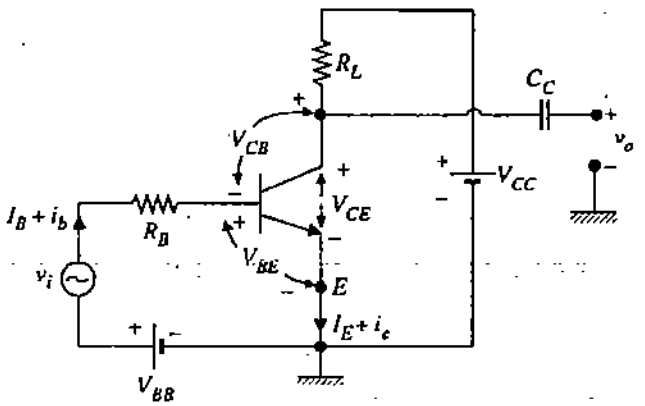


Fig. 3.27: A common emitter *npn* BJT circuit.

The common emitter configuration circuit is shown in Fig. 3.27. Here emitter has been used as the common terminal (reference). It is the most often used

configuration (because of large current gain) and is regarded as the basic configuration.

The input or $V_{BE} - I_B$ characteristic of an *npn* BJT for a fixed value of $V_{CE} (> 0.7)$ is shown in Fig. 3.28 (a). It is essentially the same as I-V characteristic of a forward biased p-n junction diode. The output $V_{CE} - I_C$ characteristic curves, one for each value of base current I_B are shown in Fig. 3.28 (b). This device has wide applications in amplifying & Oscillatory circuits which are discussed in great detail in Units 4, 5 and 6.

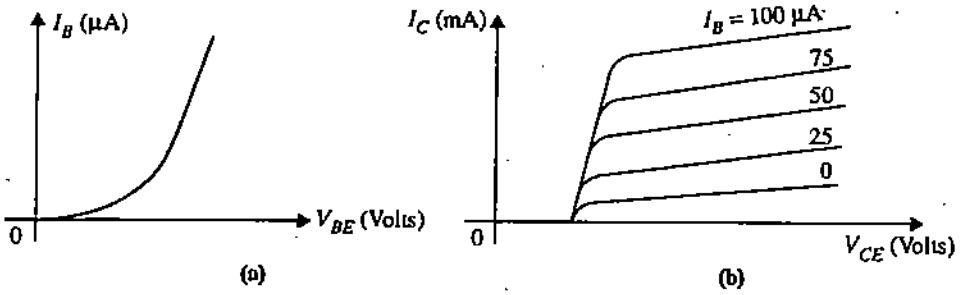


Fig. 3.28: (a) $V_{BE} - I_B$ input CE characteristic for *npn* transistor (b) $V_{CE} - I_C$ output CE characteristic for *npn* transistor.

3.5.1 Field Effect Transistor (FET)

The operation of a junction field effect transistor can be demonstrated using Fig. 3.29 (a to e). Let us consider a sample of *n*-type semiconductor. The *n*-channel presents a resistance R_{DS} as shown in Fig. 3.29 (a & b).

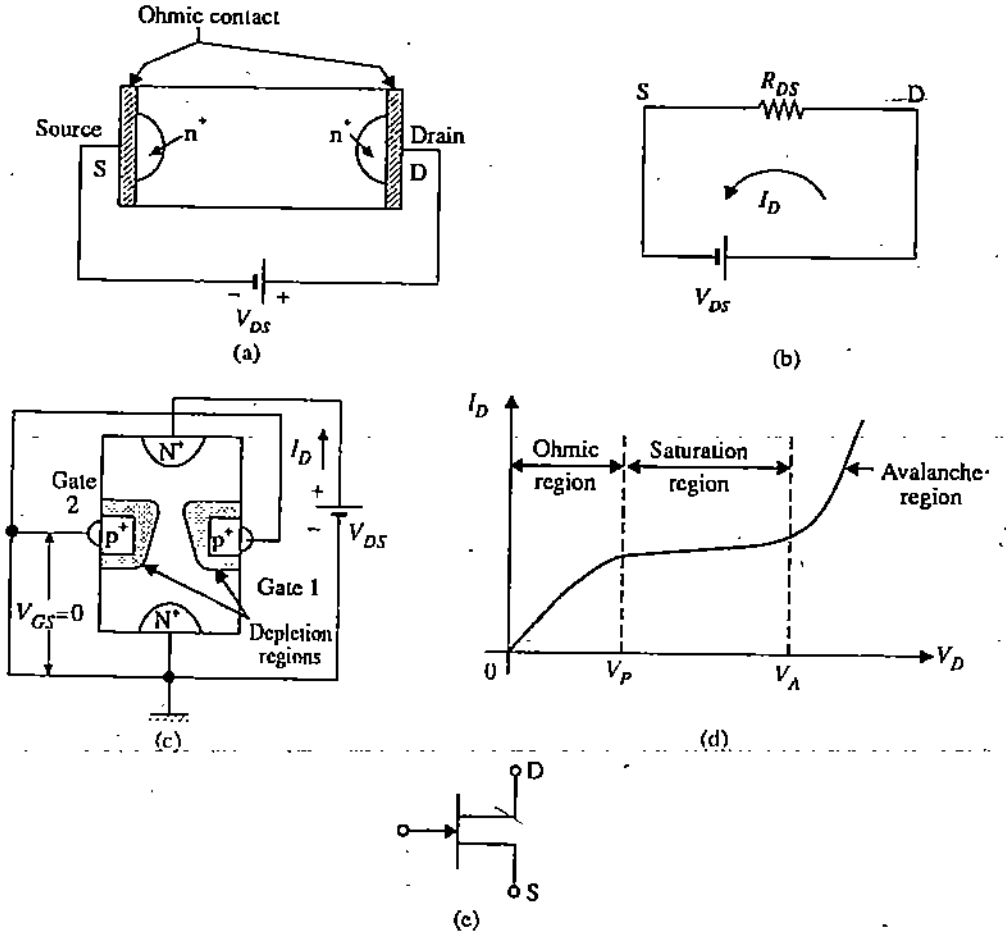


Fig. 3.29: (a) *n*-channel (b) equivalent circuit (c) structure of junction field effect transistor (d) drain characteristic of JFET (e) symbol of *n*-channel JFET.

The ohmic contacts on each side of the channel are used for making external connection. The *n*-material is doped heavily near the regions adjacent to the ohmic contacts for "Source" and "drain". The symbol n^+ in Fig. 3.29 (a) indicates the more heavily doped regions. If an external voltage is applied, the majority carriers enter the channel through the terminal called source(S). The carriers flow through the channel and leave it through the terminal called drain (D). The drain current (I_D) is equal to the majority carrier current flowing through the channel. The equivalent circuit shown in Fig. 3.29 (b), obeys ohm's law. If V_{DS} is increased, I_D increases proportionately.

Let us now diffuse *p*-type impurity so that heavily doped p^+ regions are formed on each side of the *n*-channel as shown in Fig. 3.29 (c). The ohmic contacts known as Gate 1 and Gate 2 are added to each p^+ region. The two gates are normally electrically connected together internally and only one gate terminal is made available externally. The voltage applied between gate and source (V_{GS}) controls the width of the channel; consequently the conductance of the channel and hence the drain current also vary with V_{GS}. Let both the gates be directly connected to the source so that $V_{GS} = 0$. The voltage drop in the channel due to the flow of I_D is of such polarity that it makes the *p-n* junction reverse biased. Hence, a depletion region is formed. The deplection region width increases with the magnitude of reverse bias. The reverse bias between *p*-type gate and *n*-type channel is zero near the source end and maximum near the drain end. So the depletion region is much wider and extends more into the channel near the drain end. Thus we get wedge shaped channel. The flow of electrons from source to drain is now restricted to the narrow channel between the non conducting depletion regions. The width of the channel determines the resistance between the drain and the source.

Let us consider I-V characteristic of the JFET shown in Fig. 3.29 (d). With $V_{GS} = 0$, if V_{DS} is gradually increased, I_D at first increases as ohm's law and begins to level off gradually. When V_{DS} equals V_p known as "Pinch-off voltage", I_D saturates and does not increase any further with increase in V_{DS}. At pinch off, both the depletion regions close up causing a constriction of the channel which results in high channel resistance. Any further increase in V_{DS} is absorbed as the voltage drop in the constricted region of the channel. As with all *p-n* junctions, avalanche's breakdown occurs at $V_{DS} = V_A$ and the current I_D increases rapidly. The symbol of *n*-channel JFET is shown in Fig. 3.29 (e). We can also have *p*-channel JFET.

The JFET has an edge over both vacuum tubes and BJT in that it combines the advantages of the high input impedance of vacuum tubes and the other advantages of a semiconductor device.

3.5.2 MOSFET (Enhancement & Depletion Type)

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) can be explained using Fig. 3.30 (a). A *p*-type substrate serves as the basic structure into which *n*-type regions are diffused. An oxide layer which acts as an insulator is grown over the entire substrate and the *n*-region. After etching suitable openings through the oxide, metal contacts for source and drain connections are made to the *n*-regions. No current can flow from the source to the drain because the *n*-type source, *p*-type substrate and *n*-type drain behave as two diodes connected back to back and hence no current can flow irrespective of any polarities. The gate contact is formed on the surface of the oxide layer so that gate is electrically insulated from both the substrate and *n*-regions.

Suppose we apply a positive potential between gate and the source as shown in Fig. 3.30 (b). Since oxide layer is an insulator sandwitched between conductive regions, an equivalent capacitance is formed as shown in Fig. 3.30 (c). Whenever a

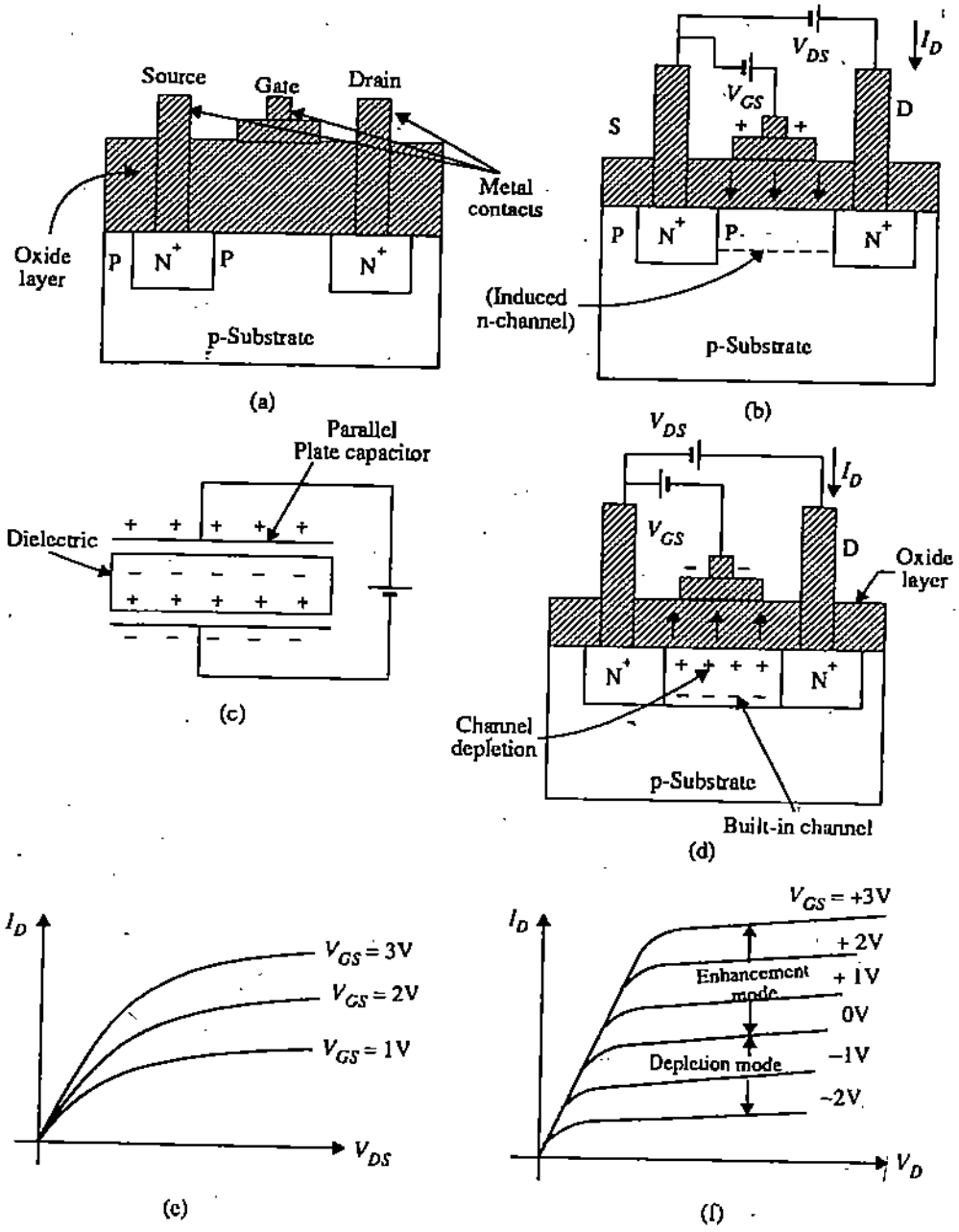


Fig. 3.30: (a) Structure of enhancement mode MOSFET (b) biasing of *n*-channel MOSFET (c) capacitor action (d) structure & biasing of depletion mode MOSFET (e) drain characteristic of enhancement type MOSFET (f) drain characteristics of depletion mode MOSFET.

positive charge is applied to one plate of a capacitor, a negative charge is induced on the opposite plate due to the action of the electric field in the dielectric, which gets polarised. So, positive charge on the gate induces a negative charge in the *p*-substrate. The charge is contributed by the electrons, which are minority carriers in the substrate and are attracted towards the area below the gate. As the number of electrons reaching this area increases, the relative density of the majority carriers decreases until there are more free electrons than holes.

Thus in relatively small region of the substrate, directly below the gate an *n*-type inversion layer is induced, which extends from source to drain and allowing conduction path between source and drain. If the positive gate potential is removed, the induced channel will disappear and there will be no conduction again. Thus the gate voltage controls the conductivity of this device. This device is known as "Enhancement type MOSFET" as the channel conductivity is enhanced by the gate potential. The input impedance working into the gate is very high since oxide layer.

behaves as an insulator. If V_{GS} is kept constant and V_{DS} is increased the drain current increases, linearly for small valuses of V_{DS}. As V_{DS} is increased further, the drop across the channel increases and hence voltage across the gate oxide at the drain end of the channel decreases. Therefore, the induced charges at this end of the channel decreases and finally the channel is pinched off i.e. there is high resistance region formed at the drain end due to paucity of induced carriers. The drain current hence tends to saturate and remain constant.

It is also possible to produce "depletion-type MOSFET". In this device there is a built in *n*-type channel. As the gate voltage increases, the channel is depleted of the carriers thus increasing the resistance as shown in Fig. 3.30 (d). If negative V_{GS} is applied, the negative charge on the gate induces an opposite and equal positive charge on the other side of the oxide layer. The recombination of the induced holes with electron in the built-in *n*-channel reduces the conductivity of the channel. As V_{GS} is made negative, I_D decreases considerably as shown in Fig. 3.30 (f). If a positive V_{GS} is applied, negative charges are induced in the *n*-channel. This enhances the channel conductivity and I_D increases. Thus, this device can be operated both in "enhancement" and "depletion" mode.

SAQ 22. Explain how a BJT can be considered as two *p-n* junctions connected back to back.

SAQ 23. In common base configuration, the current gain is less than unity, and yet the BJT is called an ampliying device. Justify.

SAQ 24. Why is β_F more than α_F ?

SAQ 25. Explain the formation of a wedge shaped channel in JFET ?

SAQ 26. Distinguish between enhancement and depletion type MOSFET 'S ?

SAQ 27. Explain how amplification is achieved in JFET and MOSFET.

3.6 SUMMARY

- The intrinsic semiconductors, germanium and silicon, can be doped to become either *p*-type or *n*-type extrinsic semiconductors.
- The majority carriers, holes in *p*-type and electrons in *n*-type material, move under the influence of an electric field to constitute a current in semiconductors.
- Noteworthy and useful properties arise when *p*-type and *n*-type materials make a *pn* junction. (A single *pn* junction is a diode).
- Holes and electrons diffuse to establish a depletion region. The charges in the regions adjacent to the depletion region generate a potential difference across the junctions.
- Two basically different kinds of transistors are made with semiconducting materials.
- The bipolar-junction transistor is formed by two *pn* junctions back to back, enclosing a very thin common element (the base). The current from the emitter to the base governs the much larger emitter-collector current, which leaks through the base.
- The field-effect transistor has a channel from source to drain, in which majority carriers move.
- In the junction field-effect transistor (JFET), the electric field from the gate modifies the depletion region in the *pn* junction between the gate and channel to control the current through the channel.

- In metal-oxide-semiconductor field-effect transistors (MOSFETs), the gate is insulated from the channel carrying the majority carriers.
- The depletion MOSFETs govern the current by depleting the channel of majority carriers.
- In enhancement MOSFETs the electric field from the insulated gate induce majority carriers into the region between the source and the drain to provide the current.

3.7 TERMINAL QUESTIONS

1. Explain the importance of space charge limited operation in thermionic vacuum tube devices.
2. Why is the introduction of third electrode (grid) in vacuum triode considered a land mark in electronics? Explain.
3. Write Note on : Tetrode, Pentode.
4. What is depletion region? Which mechanism, drift or diffusion, is responsible for the major portion of the forward current in a diode?
5. Give significance of each portion in V-I characteristic of *p-n* junction diode.
6. Draw V-I characteristic of a Zener diode.
7. Draw circuit diagrams of half wave, full wave and bridge rectifiers. Explain the operation of each and compare their performance.
8. How is drain current controlled in an Enhancement MOSFET, a depletion MOSFET and a JFET?

3.8 SOLUTIONS AND ANSWERS

SAQs

1. Example of elemental semiconductors : Silicon, Germanium.
   Example of compound semiconductors : GaAs, CdTe, GaSb.
   Example of oxide semiconductors: Tinoxide, Yittriun Barium Copper oxide.
   The conductivity of oxide semiconductors can be changed by changing the oxygen stoichiometry in oxides.
2. Work function : The amount of energy required at absolute zero temperature which must be given to the free electrons to enable it to escape the metal is defined as work function.

   Thermionic Emission : A metal is made up of atoms bound in the crystal lattices, of electrons bound to the atoms, and of free electrons that are not bound to any particular locations in the metal. In thermionic emission, the electrons are emitted when a metal is supplied with thermal energy.
3. Space charge limited operation: In all thermionic vacuum tubes, the electron emission from the cathode is at much higher rate than that at which the electrons are drawn away by the anode, resulting in a cloud of electrons near cathode, called negative space charge, makes the anode current dependent on the anode potential and independent of the rate of emission.

   In a triode, the adverse effect of space charge limited operation is taken care of by the presence of "grid", a mesh-like structure.

4. See Fig.3.2 of the text and definition of r_p, g_m and μ.

5. See small signal model in the text.

6. See section 3.2.4 of the text.

7. See section 3.3.1 and 3.3.2 of the text.

8. See section 3.3.2 (Law of mass action).

9. $n_i = A_o T^{3/2} \exp\left(\frac{-q E_g}{2KT}\right)$

   where A_o and E_g are material constants, K-boltzman's constant.

10. See section 3.3.3 of the text

11. See Fig.3.9 and use section 3.3.3 to answer this question.

12. See section 3.3.3 of the text.

13. Due to application of high electric field, the drift velocity approaches the thermal velocity ($\simeq 10^7$ cm/s). When this situation arises, the mobility becomes field dependent as additional scattering mechanisms come into play. The decrease in mobility with high electric field causes saturation of drift velocity.

14. When a p-n junction is formed, because of the concentration gradient, holes from p-side diffuse into the n-side and recombine with free electrons. Similarly, electrons from n-side diffuse to the p-side and recombine with holes. Such an exchange of mobile carriers occurs mainly in a narrow region around the junction. This region is called "depletion layer" as it becomes depleted of the free charge carriers, leaving behind unneutralised immobile ions called space charge (due to positive ions on the n-side and negative ions in the p-side). Such a space charge causes a potential difference called "barrier potential".

15. See section 3.4.1 of the text.

16. Ripple factor = $\frac{\text{rms valuse of ac component of load voltage}}{\text{dc component of load voltage}}$

    Form Factor = $\frac{\text{rms value of load voltage}}{\text{dc component of load voltage}}$

    PIV : During negative half cycle, diode acts as open circuit, and hence the negative inverse voltage appears across the diode and the maximum inverse voltage is called "Peak Inverse Voltage".

17. See section 3.4.2 (half wave rectifier) of the text.

18. See section 3.4.2 (full wave rectifier) of the text. It answers both the parts of the question.

19. **Full wave rectifier** : Ripple factor 0.482, From factor 1.11 and PIV = 2 V_m

    Bridge rectifier : (1) can be used for floating output terminal i.e., no output terminal grounded (2) Ripple factor = 0.482, From factor 1.11, PIV = V_m

20. See text page 91.

21. See text page 91.

22. A transistor can be regarded as back to back connected diode as shown in Fig. 3.31

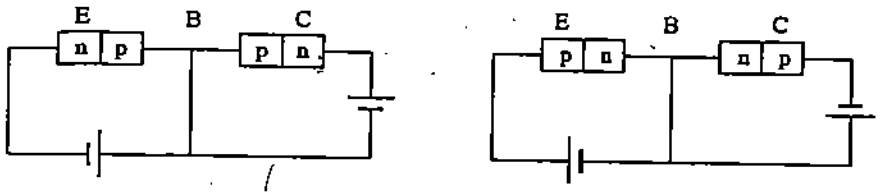


Fig. 3.31

23. Although in common base configuration, the current gain is less than unity. The voltage gain is very high and hence power gain is high. This is the reason, why BJT is called amplifying device even in CB configuration.

24. The relationship between β_F and α_F are given by ;

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

$$\Rightarrow \beta_F > \alpha_F$$

as because $\alpha_F < 1 \Rightarrow \frac{1}{1 - \alpha_F} > 1$

25. See section 3.5.1 of the text.

26. In Enhancement type MOSFET, the channel conductivity is enhanced by the gate potential. Wheras in depletion type MOSFET, as the gate potential is increased, the built-in *n*-channel is depleted of the carriers and thereby its conductivity decreases.

27. See section 3.5.1 and 3.5.2 of the text.

TQs

1. See answer of SAQ 3 and also section 3.3.2 of the text.

2. In a vacuum diode, the major problem one encountered was due to presence of space charge limited operation. This problem was taken care of by introducing a mesh like structure in the negative space-charge region nearer to the cathode. This was called "control grid". As control grid is much near to the cathode, a much smaller voltage applied to the control grid can result in the same change of anode current as will be produced by a much larger voltage applied to the plate of the tube. This forms the basis of amplifying action of triode and hence it is considered a landmark in the electronics.

3. See section 3.2.4 of the text.

4. See answer of SAQ 14.

Majority carriers, which are responsible for large forward current in a *p-n* junction diode, mainly contribute to the drift current.

5. See section 3.4.1 of the text.

6. See section 3.4.2 (iii) of the text.

7. See section 3.4.2 (i) of the text.

8. See section 3.5.2 of the text.

NOTES

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Utter Pradesh
Rajarshi Tandon Open University

Block

2

ELECTRONIC CIRCUITS

BLOCK 2 ELECTRONIC CIRCUITS

In the previous Block you have studied about dc and ac circuit theory. You were also introduced to various electronic devices. Using the characteristics of transistor described in Unit 3 and the circuit theory of Unit 2, we are now ready to study the analysis and design of various types of electronic circuits used in amplifiers, oscillators and power supplies.

The most important property of the semiconductor is their ability to function as amplifiers of electrical voltage, current or power. When voltage or current signals are applied to the input terminals of an amplifier, larger voltage or current signals are available at the output terminals.

In Unit 4 our approach is first to look at the practical considerations in amplifier operation and devise circuits for maintaining the proper operating conditions, then to analyze the performance of one type of power amplifier and finally to describe briefly some other important types of amplifiers.

Sometimes, it becomes necessary to generate alternating currents of high frequencies (ranging upto millions and even billions of cycles per second). As we shall see, transistors together with associated components, may be used to generate these currents. We call such generators as oscillators. Unit 5 discusses a variety of sinusoidal oscillators include RC oscillators and LC oscillators.

In all previous units, the voltages and currents required to operate the analog circuits were assumed to be available . Now we will examine how currents and voltages are provided and the means by which they are regulated; that is, how they are kept within the precise magnitudes that are desired. Most electronic circuits need a dc voltage in order to work properly. Since line voltage is alternating , the first thing that has to be done in any electronic equipment is to convert ac voltage to dc voltage. The aim of Unit 6 is to explain how well-regulated dc power supplies for electronic circuits can be derived from the ac mains.

UNIT 4 AMPLIFIERS

Structure

4.1 INTRODUCTION

You are all familiar with an 'audio system' which is used to play records, play and record audio tapes, and receive radio broadcasts. Fig. 4.1a shows a simple diagram for such a

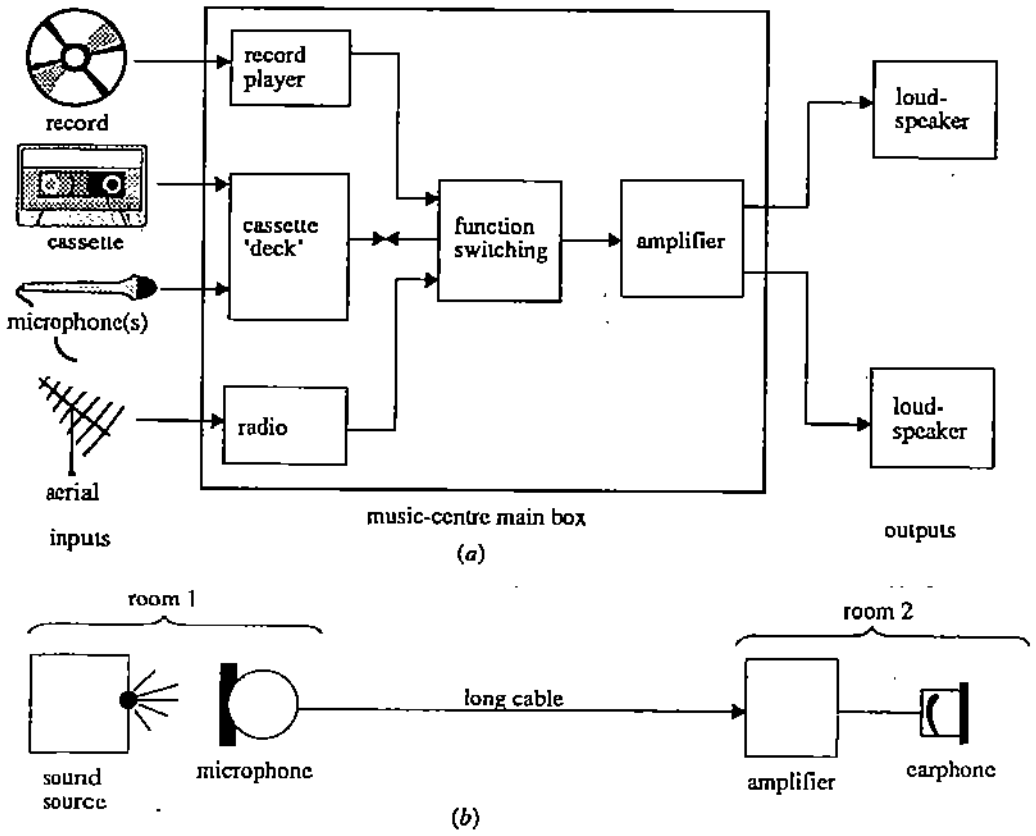


Fig. 4.1: (a) A Simple block diagram for an audio system. (b) The simple audio system.

system. For simplicity, suppose the 'audio system' of Fig. 4.1 performs only one of the functions, in that case the diagram of the 'simple audio system' will be as shown in Fig. 4.1(b). It consists of a microphone connected to the input of an amplifier whose output is connected to the loudspeaker. The microphone converts sound into electrical signals. The loudspeaker carries out the reverse process by converting electrical signals into sound. Without the amplifier, the electrical output of the microphone is too weak to provide a comfortable sound level in the loudspeaker. The amplifier is used to convert the microphone output into a sufficiently powerful electrical signal for the loudspeaker.

Fig.4.1 do not show a power supply but you must know that electronic systems need such a supply. They may either be provided with batteries or plugged into the mains to make them operate. In that case Fig.4.1 look something like Fig.4.2(a). Here the amplifier controls the flow of power from the power supply to the loudspeaker in response to the electrical signal received from the microphone. When the sound enters the microphone, it generates an output voltage. Since the voltage and the current flowing are relatively small, the product (voltage × current) i.e., power is relatively small. But the microphone signal voltage causes the amplifier to allow power to flow, from the power supply, to the loudspeaker. In this way amplifier helps to supply much more signal power to the loudspeaker than the microphone can provide.

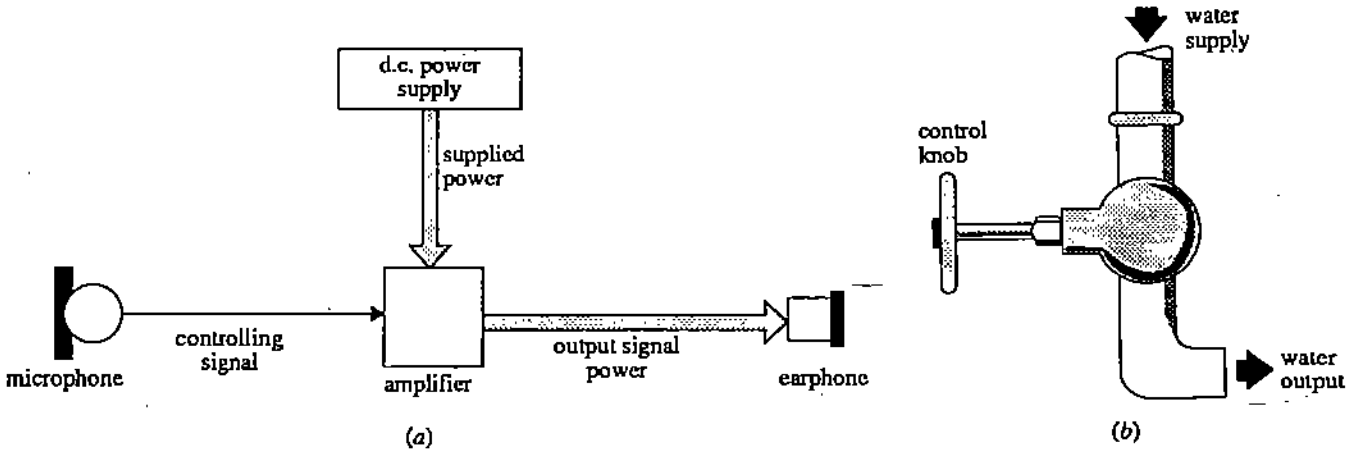


Fig. 4.2: (a) Power flow in the audio system. b) A water-tap analogy of an amplifier.

This can be thought of as being analogous to the control of water through a tap, as shown in Fig.4.2 (b). Here the 'controlling signal' is fed in at the position of the control knob, and this determines the flow of water from the mains supply through the tap.

The central 'black box' of the Fig.4.1 or 4.2(a) is the amplifier whose only function is to increase (boost) the level of the signal. These amplifier circuits may use electron tubes or transistors since both are essentially amplifying devices. Amplifier circuits can be classified in a wide variety of ways. In this unit we will mention the various types of amplifier within each of these classification.

Also, in this unit you will learn in detail what happens when a small signal and when a large signal is given to the input terminal of the amplifier. You will see the difference the magnitude of the input signal is going to make on the output signal. Further in small signal applications you will learn about the gain, band width and input and output resistances of the amplifier. Finally at the end, various types of large signal amplifiers, their merits and demerits are going to be discussed. But before discussing this you should be familiar with the terms such as equivalent circuit of transistors, operating point, bias stability etc.

In the next unit we will see how the introduction of feedback in the amplifier circuit makes it into a useful device called oscillator. We will also study different types of oscillator.

Objectives

After going through this unit you will be able to :

- compare the CE, CB and CC configurations in amplifier circuits.

- state the classification of amplifiers on the basis of purpose, operating point, coupling, circuit configuration, band width and frequency,
- calculate the current gain, voltage gain, input impedence and output impedence for amplifier circuits, by using *h* parameters,
- draw different biasing arrangements in transistor circuits,
- explain with the help of simple equations as to why the potential divider biasing circuit is the most widely used circuit,
- calculate the overall gain of multistage amplifier, if the gain of each stage is known,
- describe the frequency response curve of an RC coupled amplifier,
- sketch single ended and push pull amplifier circuits,
- determine the output ac power developed in a single-ended power amplifier, when supplied with various parameteres,
- explain the working of push-pull amplifier circuit,
- explain the working of single tuned voltage amplifier and double-tuned amplifier.

4.2 CLASSIFICATION OF AMPLIFIERS

Amplifier circuits can be classified in a wide variety of ways. They can be classified according to their use, the type of bias used, the **frequency** or **bandwidth** of the signals they are to amplify, the type of coupling , if more than one stage is used, and their circuit configuration.

Amplifiers according to use: They fall into two main groups : Voltage amplifiers and power amplifiers. Voltage amplifiers increase the voltage level of an applied signal. Since the output voltage of an amplifier is determined by the voltage drop across the output lead, the impedence of the load is made as large as is practical in most voltage amplifiers.

Power amplifiers are also called current amplifiers. They deliver a large amount of current to the output load so that the load impedence is usually low enough to allow a high current output.

Amplifiers according to bias: Amplifiers are also classified according to their biasing conditions, or, in other words, according to the portion of the input signal voltage cycle during which output current flows. There are four classes of amplifiers according to bias: class A, class B, class AB and class C.

Class A amplifiers are biased in the center of their operating curves so that output current flows during the entire cycle of the input voltage(see Fig.4.3a). This results in minimum distortion of the output signal, and, as a result, class A amplifiers are widely used in audio systems, where low distortion is important.

Class B amplifiers are biased at cutoff so that output current flows for approximately one-half of the input signal voltage cycle as shown in Fig.4.3(b) . When no input signal is present, no output current flows. In effect, a class B amplifier cuts off one half of the a-c input signal waveform.

Class AB amplifiers are biased so that output current flows for appreciably more than one half of the input cycle, but for less than the entire cycle as shown in Fig.4.3(c). Essentially, class AB amplifiers are a compromise between the low distortion of class A amplifiers and the high efficiency of class B amplifiers.

Class C amplifiers are biased beyond cutoff so that output current only flows during the positive going peak of the input cycle (see Fig.4.3d). Such, amplifiers have high power outputs. They also have a high degree of distortion, which prevents their use in audio applications.

Amplifiers according to coupling: Where more than a single amplifier stage is used, the amplifiers are often classified according to the way in which they are coupled. The basic coupling methods are: resistance-capacitance (RC) coupling, impedence coupling, transformer coupling and direct coupling. In RC coupling, the output load is a resistance.

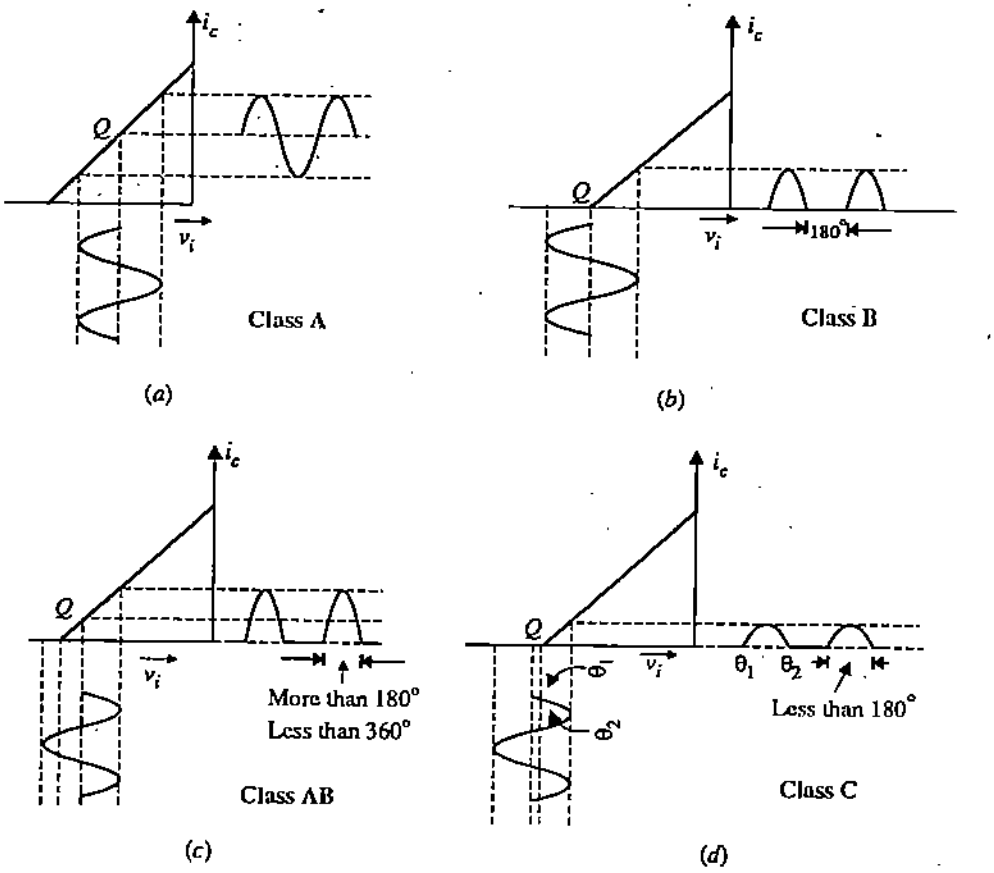


Fig. 4.3: Classification of amplifier according to bias.

In impedence coupling, a coil is used as the output load instead of a resistance. In transformer coupling the output of one circuit is coupled to the input of the next by means of a transformer. In direct coupling, the output of one stage is applied directly to the input of the next stage.

Amplifiers according to circuit configuration: Amplifiers are classified on the basis of the principal elements returned to ac ground. These are:

(i) grounded base or common base (CB) amplifier.

(ii) grounded-emitter or common emitter (CE) amplifier

(iii) grounded collector or common collector (CC) amplifier.

Amplifiers according to band width: There are two principal types of amplifiers : those that are **tuned** and amplify a restricted range of frequencies and those that are **untuned** and amplifies a wide range of frequency.

Amplifiers according to frequency: They are classified as direct current (d-c) amplifier, audio frequency (a-f) amplifier, intermediate frequency (if) amplifier, radio frequency (r-f) amplifier and video frequency (v-f) amplifier. As their names imply, d-c amplifiers amplify signals of very low frequency. Audio amplifiers operate in the audio frequency range i.e. from 20 to 20,000 cycles per second. Video amplifiers amplify signals from the lower audio frequencies to as high as 4 or 5 mega cycles per second.

I-f and r-f amplifiers are not defined in terms of a specific frequency range. Instead, they are defined by the nature of the frequencies they amplify. Generally, they are tuned amplifiers, and therefore amplify a relatively small band of frequencies. I-f amplifiers operate at the intermediate frequency of a particular piece of equipment, and r-f amplifiers are tuned to the frequencies of various r-f carrier waves.

You will find that this method of grouping amplifiers is somewhat arbitrary, in as much as all of the methods of classification overlap to some degree. For instance, audio amplifiers may also be voltage or power amplifiers. Similarly, an r-f amplifier is usually a tuned amplifier, and at the same time may be a common emitter or common base amplifier. In spite of this overlap, for purposes of description, some grouping must be used.

4.3 EQUIVALENT CIRCUIT OF TRANSISTOR

In Unit 3 you have learned about different electronic devices. When you use them for some application and you want to analyze the circuit it is not possible to do so without replacing these devices by some equivalent circuit. Therefore, in this unit we will discuss how this could be done for a transistor. Further you have to supply appropriate voltages to the different elements and the device must operate linearly. So we will also discuss about the operating point and stability.

A transistor equivalent circuit is basically a circuit consisting of ideal voltage and/or current "sources" or "generators" and passive components (R,L and C), which acts electrically exactly like the transistor. In other words, the transistor can be replaced by an appropriate collection of generators and passive components of the equivalent circuit. The advantage of the equivalent circuit is that one can predict the transistor's exact behaviour (gain,etc.) by writing down the Kirchhoff voltage and current laws for the various loops and junctions and solving for the desired quantities by using only algebra and Ohm's law. A simple example will show how the calculations are performed. Suppose a certain transistor's equivalent circuit is simply an ideal voltage generator of magnitude Av_{in} in series with a resistance R as shown in Fig.4.4.

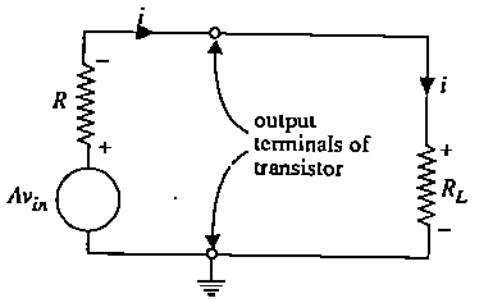


Fig. 4.4: Simple equivalent circuit.

Algebraically, A is a positive number, and v_{in} is the amplitude of the input voltage to the transistor. The R_L is the load resistance connected to the output terminals. The voltage generator produces a voltage A times as large as the input , so one might intuitively think of A as the voltage gain at this stage of the calculation. However, the voltage gain is

$$A_v = \frac{v_{out}}{v_{in}} = \frac{iR_L}{v_{in}} \tag{4.1}$$

and the current i can be obtained from the Kirchhoff voltage equation for the loop containing the generator, R, and R_L.

$$Av_{in} - iR - iR_L = 0$$

or
$$i = \frac{Av_{in}}{R + R_L} \tag{4.2}$$

Thus the voltage gain becomes

$$A_v = \frac{V_{out}}{V_{in}} = \frac{iR_L}{v_{in}} = \frac{Av_{in}R_L}{(R+R_L)v_{in}}$$

or
$$A_v = A\left(\frac{R_L}{R+R_L}\right) \tag{4.3}$$

We see that the voltage gain depends on A, R, and R_L, and only as R_L becomes very large compared to R we get $A_v \cong A$.

Let us now develop a perfectly general equivalent circuit that will apply to any four-terminal device, as shown in Fig.4.5(a). I_1 and I_2 are the currents flowing into the input and output, respectively, and V_1 and V_2 are the voltage differences across the input

and the output terminals, respectively. We have four variables : I_1 , V_1 , I_2 and V_2 ; they present the total, instantaneous values of the currents and voltages.

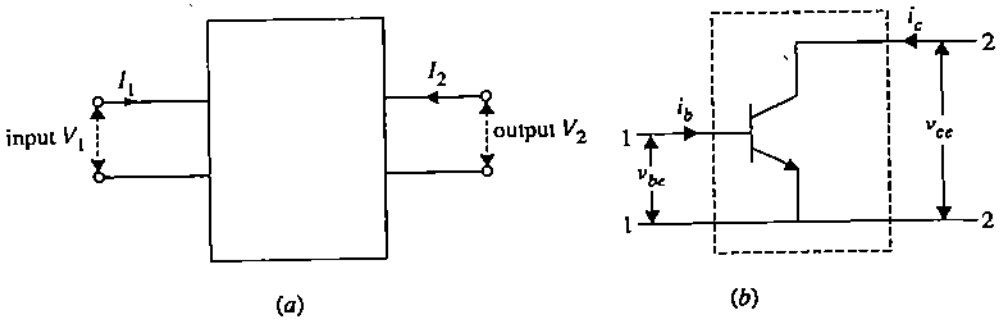


Fig. 4.5: (a) General four-terminal black box. (b) Transistor as a four-terminal network.

A transistor has three terminals, whereas our black box from which the equivalent circuit is developed has four. Hence, for the equivalent circuit to be applied to a transistor, one transistor terminal must be common between the input and output. This can either be the emitter, the collector or the base called respectively the "common emitter" (CE), "common collector" (CC) or the "common base" (CB) configurations.

Any network having a pair of input terminals and a pair of output terminals is called a two part network or a four terminal network. A transistor in the "common emitter" (CE), the "common base" (CB) or the "common collector" (CC) configuration can also be treated in a similar way, as shown in Fig.4.5(b). 1,1 are the input terminals and 2,2 are the output terminals, i_b and v_{be} are the input current and input voltage while i_c and v_{ce} are the corresponding values of the output circuit. Thus, we have four quantities two of which are currents and two of them are the voltages. Of these four quantities we can take two of them dependent quantities and the other two as independent quantities. Thus we express the dependent quantities in terms of independent ones. Selection of these quantities give different equivalent circuits for the four-terminal network. However, for a transistor, an equivalent circuit by the selection if i_b and v_{ce} as independent and i_c, v_{be} as dependent. is widely used due to the simplicity involved. Thus we write

$$i_c = f(i_b, v_{ce}) \tag{4.4}$$

and

$$v_{be} = (i_b , v_{ce}) \tag{4.5}$$

If we consider, Fig.4.5(a), then,

$$I_2 = I_2(I_1, V_2) \tag{4.6}$$

$$V_1 = V_1 (I_1, V_2) \tag{4.7}$$

In general, we are interested in the response of the transistor to ac signals, so we will take the differential of (4.6) and (4.7) to obtain expressions for the change in I_2 . (*i.e.* dI_2) and the change in V_1(*i.e.* dV_1)

$$dI_2 = \left(\frac{\partial I_2}{\partial I_1}\right)_{V_2} dI_1 + \left(\frac{\partial I_2}{\partial V_2}\right)_{I_1} dV_2 \tag{4.8}$$

$$dV_1 = \left(\frac{\partial V_1}{\partial I_1}\right)_{V_2} dI_1 + \left(\frac{\partial V_1}{\partial V_2}\right)_{I_1} dV_2 \tag{4.9}$$

Let us change to a notation useful for considering ac signals or any change in the currents and voltages. Let $i_2 = dI_2$, $i_1 = dI_1$, $v_1 = dV_1$ and $v_2 = dV_2$. That is, lowercase v's and i's refer to changes in the voltages and currents or, equivalently, to ac signal amplitudes. With this notation,

$$i_2 = \left(\frac{\partial I_2}{\partial I_1}\right)_{V_2} i_1 + \left(\frac{\partial I_2}{\partial V_2}\right)_{I_1} V_2 \tag{4.10}$$

$$v_1 = \left(\frac{\partial V_1}{\partial I_1}\right)_{V_2} i_1 + \left(\frac{\partial V_1}{\partial V_2}\right)_{I_1} v_2 \tag{4.11}$$

We now define the h parameters for our four-terminal black box in terms of the partial derivatives:

$$h_{21} = h_f = \left(\frac{\partial I_2}{\partial I_1}\right)_{V_2} = \frac{I_2}{I_1} = \text{short circuit forward current ratio, } V_2 = 0$$

$$h_{22} = h_o = \left(\frac{\partial I_2}{\partial V_2}\right)_{I_1} = \frac{I_2}{V_2} = \text{open circuit output admittance, } I_1 = 0$$

$$h_{11} = h_i = \left(\frac{\partial V_1}{\partial I_1}\right)_{V_2} = \frac{V_1}{I_1} = \text{short circuit input impedence, } V_2 = 0$$

$$h_{12} = h_r = \left(\frac{\partial V_1}{\partial V_2}\right)_{I_1} = \frac{V_1}{I_1} = \text{Open circuit reverse voltage ratio, } I_1 = 0$$

Table 4.1 summarizes the meaning of each h parameter and the required condition.

Table 4.1: h Parameters.

Parameter	Meaning	Equation	Condition
h_{11}	Input impedance	$\frac{V_1}{I_1}$	Output shorted
h_{12}	Reverse voltage gain	$\frac{V_1}{V_2}$	Input open
h_{21}	Current gain	$\frac{I_2}{I_1}$	Output shorted
h_{22}	Output admittance	$\frac{I_2}{V_2}$	Input open

The h parameters have a variety of dimensions; hence the name "hybrid" parameters. With this notation we have

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2 \tag{4.12}$$

$$i_1 = h_{11}\, i_1 + h_{12}\, v_2 \tag{4.13}$$

Eqs. (4.12) and (4.13), relating the dependent variables i_2 and v_1 to the independent variables i_1 and v_2 via the h parameters, determine the equivalent circuit. The term $h_{21}\, i_1$ means there is a current generator of magnitude h_{21} times i_1. The term $h_{22}\, v_2$ means the voltage v_2 appears across a conductance h_{22} (or equivalently accross a resistance of $\frac{1}{h_{22}}$ ohms). The term $h_{11}\, i_1$ means the current i_1 flows through an effective resistance of h_{11} ohms. The term $h_{12}v_2$ means there is a voltage generator of magnitude $h_{12}v_2$. Therefore, we can draw the equivalent circuit of Fig.4.6. Eq.(4.12) is seen merely the Kirchhoff current equation for the output, and Eq. (4.13) is merely the Kirchhoff voltage equation for the input.

Some physical feeling for the h parameters can be obtained from the equivalent circuit of Fig.4.6.

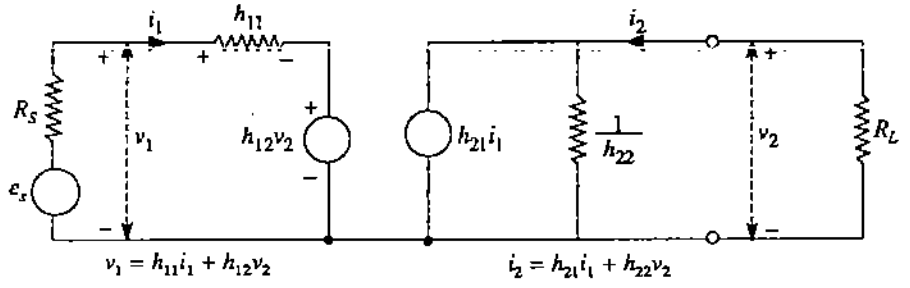


Fig.4.6: Transistor h parameter equivalent circuit.

The h_{11} parameter is a resistance in the input circuit, usually called the "input resistance". The term $h_{12}v_2$ is the amplitude of a voltage generator in the input: it represents how much of the output voltage v_2 is transferred or fed back to the input, and h_{12} is called the "reverse voltage transfer ratio". The word "reverse" is used to denote the transfer from the output back to the input. The h_{21} parameter represents how much of the input current i_1 is transferred to the output: h_{21} is called the "forward current transfer ratio". The higher the value of h_{21} is, the larger is the change in output current for a given input current change. We call h_{22} the "output admittance" because it is an admittance or conductance directly across the output terminals.

The h parameters of transistors can be listed as

$$h_i = h_{11}$$

$$h_r = h_{12}$$

$$h_f = h_{21}$$

$$h_o = h_{22}$$

where h_i = input impedance with output shorted

h_r = reverse voltage gain with input open

h_f = forward current gain with output shorted

h_o = output admittance with input open

To remember this, notice that the subscript is the first letter of the description:

i = input

r = reverse

f = forward

o = output

The h parameters of a transistor depend on the connection which is used: CE, CC, CB. Because of this the letter e is included for CE connection, c for CC connection and b for CB connection. Table 4.2 summarizes the notation for commonly used transistor h parameters. As you can see, CE parameters are h_{ie}, h_{re}, h_{fe} and h_{oe}.

Table 4.2: Relations

General	CE	CC	CB
h_{11}	h_{ie}	h_{ic}	h_{ib}
h_{12}	h_{re}	h_{rc}	h_{rb}
h_{21}	h_{ie}	h_{fc}	h_{fb}
h_{22}	h_{oe}	h_{oc}	h_{ob}

The general h parameter equivalent circuit of Fig.4.6 and Eqs.(4.12) and (4.13) are widely used to calculate the voltage gain, current gain, the input impedence and the output impedence of the transistor amplifier in its three configurations:

(i) common emitter

(ii) common base

(iii) common collector

4.3:1 Common Emitter Amplifier

Fig.4.7 shows a CE amplifier. A small sine wave is applied at the input. This produces variations in the base current. Because of β, the collector current is amplified sine wave of

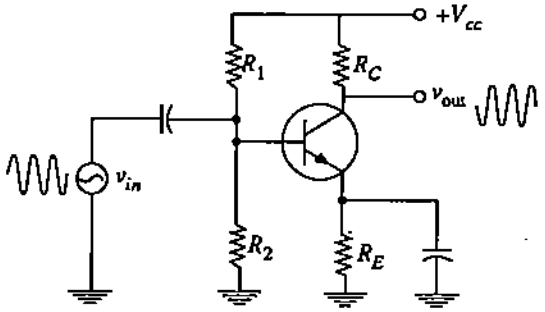


Fig.4.7: Common emitter amplifier.

the same frequency. This sinusoidal collector current flows through the collector resistance and produces an amplified output voltage.

Notice that the ac output voltage is inverted with respect to the ac input voltage, meaning that it is 180° out of phase with the input. During the positive half cycle of input voltage, the base current increases, causing the collector current to increase. This produces a larger voltage drop across the collector resistor; therefore, the collector voltage decreases, and get the first negative half cycle of output voltage. Conversely, on the negative cycle of input voltage, collector current flows and the voltage drop across the collector resistor decreases. For this reason, the collector-to-ground voltage rises and we get the positive half cycle of output voltage.

Current Gain

The current gain of an amplifier is defined as the ratio of the ac output current to ac input current. In symbols

$$A_i = \frac{i_2}{i_1} \tag{4.14}$$

With Eq. (4.12), we can rewrite Eq. (4.14) as

$$A_i = \frac{h_{21}\, i_1 + h_{22} v_2}{i_1} = h_{21} + h_{22} \frac{v_2}{i_1}$$

From Fig.4.6 you can see that $v_2 = - i_2 R_L$. When this is substituted, we get

$$A_i = h_{21} - h_{22} \frac{i_2 R_L}{i_1} = h_{21} - A_i h_{22} r_L$$

solving for A_i, we get

$$A_i = \frac{h_{21}}{1 + h_{22} r_L} \tag{4.15}$$

Voltage Gain

The voltage gain of an amplifier is defined as the ratio of ac output voltage to ac input voltage. In symbols,

$$A_v = \frac{v_2}{v_1}$$

With Eq. (4.13),

$$A_v = \frac{v_2}{h_{11}\, i_1 + h_{12}\, v_2} = \frac{- i_2 r_L}{h_{11}\, i_1 - h_{12}\, i_2 r_L}$$

Dividing the numerator and denominator by i_2 gives

$$A_v = \frac{- r_L}{h_{11}/A_i - h_{12} r_L}$$

Using Eq. (4.15) we get

$$A_v = \frac{-h_{21}\, r_L}{h_{11} + (h_{11}\, h_{22} - h_{12}\, h_{21})\, r_L} \tag{4.16}$$

Input Impedence

The input impedence of a loaded two port network is

$$Z_{in} = \frac{v_1}{i_1} = \frac{h_{11}\, i_1 + h_{12} v_2}{i_2} = h_{11} + \frac{h_{12}\, v_2}{i_1}$$

since $v_2 = -\, i_2\, r_L$.

$$Z_{in} = h_{11} - \frac{h_{11}\, i_1 + h_{12}\, v_2}{i_1} = h_{11} - A_i\, h_{12}\, r_L$$

Using Eq. (4.15), we get

$$Z_{in} = h_{11} - \frac{h_{12} h_{21}\, r_L}{1 + h_{22} r_L} \tag{4.17}$$

Output Impedence

To get the output impedence, the source voltage shown in Fig.4.6 is reduced to zero. Then drive the output terminals with a signal of v_2 as shown in Fig.4.8. The ratio of v_2 to i_2 is the output impedence of the two port network. In symbols,

$$Z_{out} = \frac{v_2}{i_2} = \frac{v_2}{h_{21}\, i_1 + h_{22}\, v_2} \tag{4.18}$$

On the input side, Ohm's law gives

$$i_1 = \frac{-\, h_{12}\, v_2}{r_s + h_{11}}$$

when this is substituted in Eq. (4.18), we get

$$Z_{out} = \frac{r_s + h_{11}}{(r_s + h_{11})\, h_{22} - h_{12}\, h_{21}} \tag{4.19}$$

Thus for a CE amplifier, the h formulas are written as follows:

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

$$A_v = \frac{h_{fe}\, r_L}{h_{ie} + (h_{ic}\, h_{oc} - h_{re}\, h_{fe})\, r_L}$$

$$Z_{in} = h_{ie} = \frac{h_{re}\, h_{fe}\, r_L}{1 + h_{oc}\, r_L}$$

$$Z_{out} = \frac{r_s + h_{ie}}{(r_s + h_{ie})\, h_{oe} - h_{re}\, h_{fe}}$$

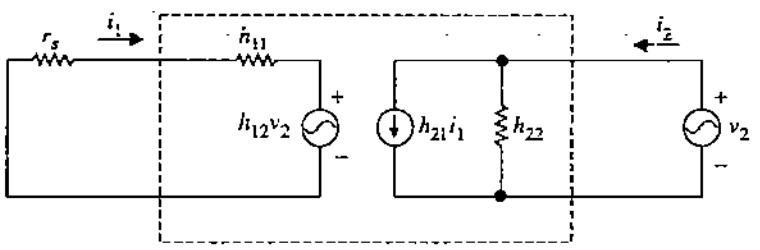


Fig. 4.8: To find output impedence, driving the output side with a signal v_2.

4.3.2 Common Base Amplifier

Fig.4.9 shows a common base amplifier. The base terminal is common to both the input and the output. The input is at the emitter, and the output is taken off the collector i.e., across the collector resistor R_C. In the common base amplifier, the output is in phase with the input. A positive input makes the emitter more positive than base, thus the collector current decreases. This decrease in the collector current causes the output voltage at the collector to rise, thus giving a positive going output.

For calculating the current gain, voltage gain, input impedence and output impedence, we need to use the CB parameters :h_{ib} , h_{rb} , h_{fb} and h_{ob}. The basic formulas become

$$A_i = \frac{h_{fb}}{1 + h_{ob}\, r_L} \tag{4.20a}$$

$$A = \frac{-\, h_{fb}\, r_L}{h_{ib} + (h_{ib}\, h_{ob} - h_{rb}\, h_{fb})\, r_L} \tag{4.20b}$$

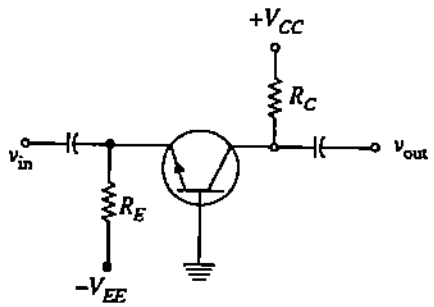


Fig. 4.9: Common base amplifier.

$$Z_{in} = h_{ib} - \frac{h_{rb}\, h_{fb}\, r_L}{1 + h_{ob}\, r_L} \tag{4.20c}$$

$$Z_{out} = \frac{r_s + h_{ib}}{(r_s + h_{ib})\, h_{ob} + h_{rb}\, h_{fb}} \tag{4.20d}$$

4.3.3 Common Collector Amplifier

In the common collector configuration shown in Fig.4.10, the collector terminal is common to both the input and the output. The input is at the base and the output is taken off the emitter, that is, across the emitter resistor R_E. As the input goes more positive, the transistor turns on and I_E increases, which means that the output also goes more positive. In other words, the output voltage is in phase with the input voltage. The common collector amplifier is thus often called the "emitter follower" because the output voltage on the emitter "follows" the input voltage at the base.

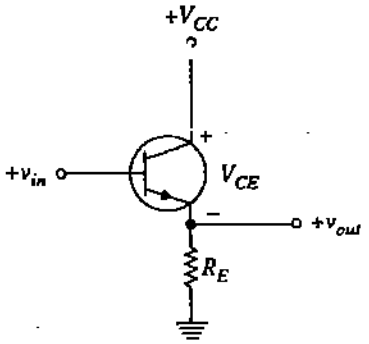


Fig. 4.10: Common collector amplifier.

To calculate the current gain, voltage gain, input impedence, output impedence we need to use the h parameters of cc connection: h_{ic}, h_{rc}, h_{fc} and h_{oc}. The following formulas are obtained:

$$A_I = \frac{h_{fc}}{1 + h_{oc} r_L} \tag{4.21a}$$

$$A = \frac{-h_{fc} r_L}{h_{ic} + (h_{ic} h_{oc} - h_{rc} h_{fc}) r_L} \tag{4.21b}$$

$$Z_{in} = h_{ic} - \frac{h_{rc} h_{fc} r_L}{1 + h_{oc} r_L} \tag{4.21c}$$

$$Z_{out} = \frac{r_s + h_{ic}}{(r_s + h_{ic}) h_{oc} - h_{rc} h_{fc}} \tag{4.21d}$$

To sum up, in Table 4.3 we give comparison among three types of amplifier circuits.

Table 4.3: Comparative study of three types of amplifier circuits.

Property	Common Emitter	Common Base	Common Collector
Transistor resistance	Medium input impedence and medium output impedence	a relatively low input impedence and a relatively high output impedence	high input impedence and low output impedence
Current gain	Large current gain	Approximately no current	Current gain is high
Voltage gain	Large voltage gain	Voltage gain is fair	Voltage gain is less than unity
Phase of input and output signals	Input and output signals are 180° apart	No phase reversal	No phase reversal
Principal use	in transistor configuration	in very high frequencies	In driving low impedence loads such as loudspeakers

4.4 OPERATING POINT AND BIAS STABILITY

In order to get optimum performance of a device, appropriate voltage have to be applied to its different elements. The voltages that you apply should be such that the device functions linearly even when a small change occurs in the applied voltage. The operating voltage and current at the output element and that of the input electrode defines the operating point or the "quiescent" point of the device. For example, for a transistor in common emitter configurations the operating point on the load line is the point that represents I_C, V_{CE} and I_D for no input signal.

When a transistor is used in amplifier circuit, a small ac signal is put into the transistor to get a larger ac signal of the same frequency. Before the ac signal can be coupled into a transistor, we have to set up quiscent (Q) point of operation, typically near the middle of the load line. Then the incoming ac signal will produce fluctuations above and below this Q point. The Q point is specified by V_{CE} and I_C, for a transistor in common emitter configuration. Therefore, for the device to function linearly, the fluctuations in current and voltage must not drive the transistor into either saturation or cut off.

Applying the appropriate voltages to the different elements of the transistor is called **biasing**. The biasing is affected by transistor parameter variations, transistor replacement, temperature etc. Making the Q-point (operating point) independent of these changes is called **stabilisation**. The biasing circuits employ dc feedback to achieve stabilization of

various biasing circuits like fixed bias (also called base bias). Self bias (also called collector feedback bias) and the universal bias (also called the voltage divider bias). Fixed bias is never used to bias a transistor for linear operation because in this case the Q-point is unstable. Fig.4.11 shows the various biasing circuits. In self-bias, the base resistor is returned to the collector rather than to the power supply. This is what distinguishes fixed bias from the self bias. This type of bias is somewhat more effective than fixed bias. Although the circuit is still sensitive to changes it is used in practice. It has the advantage of simplicity (there are only two resistors).

Universal bias is the bias most widely used in linear circuits. The name "voltage divider" comes from the voltage divider formed by R_1 and R_2. The voltage across R_2 forward biases the emitter diode.

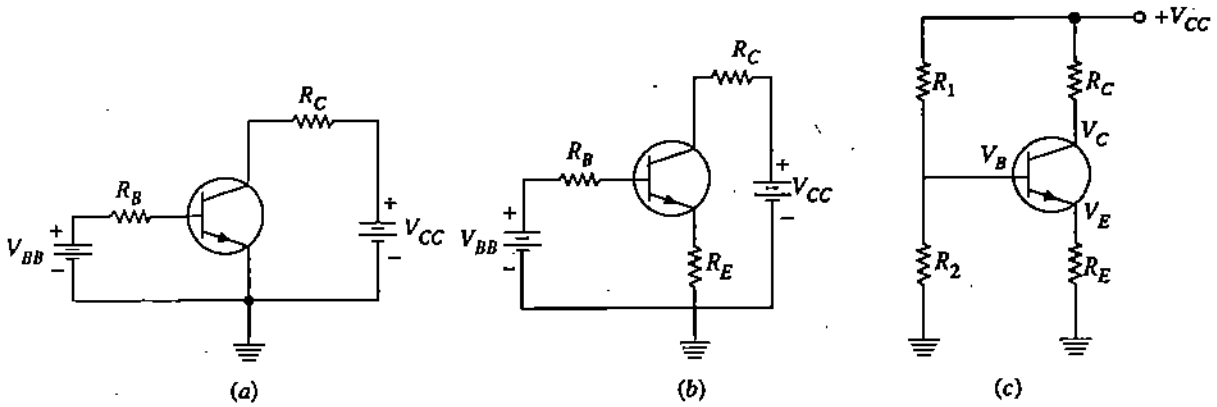


Fig. 4.11: a) Fixed bias (b) Self-bias (C) Universal bias.

You can see from Fig.4.11 (c), that we require only one battery $+V_{CC}$. It uses four resistors and provides stability of the Q-point according to the following relation :

$$I_C\uparrow \rightarrow I_E\uparrow \rightarrow (I_E\ R_E)\uparrow \rightarrow V_{BE}\downarrow$$

(since V_{R2} is constant and is equal to

$$V_{BE} + I_E R_E \rightarrow I_C\downarrow \qquad (4.22)$$

Here, arrow pointing upward shows that the physical quantity accompanying such arrow is increasing whereas the physical quantity accompanying the arrow pointing downward is decreasing in magnitude. For instance, if β_{dc} increases, the collector current increases. This increases the emitter voltage, which decreases the voltage across the base resistor and reduces the base current. The reduced base current results in less collector current, which offsets the original increase in β_{dc}.

β of a transistor is defined as :

$$\beta = \frac{I_C}{I_B},$$

Where I_C is the collector current and I_B is the base current.

Resistors R_1 and R_2 form a voltage divider across the V_{CC} supply. The current through the combinations is selected to be about $\frac{1}{10}$ th of the collector current i.e. $I_1 = I_C/10$. Since the base current is small the current through R_2 can also be taken $\sim I_1$. So the voltage across R_2 is

$$V_{R_2} = I_1 R_2 = \frac{V_{cc} R_2}{R_1 + R_2}$$

This is also $= V_{BE} + V_{RE} = V_{BE} + I_E R_E$

$$= V_{BE} + I_C R_E \qquad (\because I_C = I_E)$$

$$\therefore \frac{V_{CC} R_2}{R_1 + R_2} = V_{BE} + I_C R_E$$

Since the LHS is constant, a change in I_C causes V_{BE} to change in a direction, so as to bring I_C back to the original values refer, as shown in Eq.(4.22).

Example 1

Calculate the dc bias voltages (i.e., base voltage, emitter voltage, collector voltage and collector to emitter voltage) and currents (i.e., emitter current and collector current) for the circuit of Fig.4.11.c. Here $R_1 = 40\text{k}\Omega$, $R_2 = 5\text{k}\Omega$, $R_C = 5\text{k}\Omega$, $V_{CC} = 12\text{V}$ and $R_E = 1$. Assume $V_{BE} = 0.3\text{V}$ and $\beta = 60$ for the transistor used.

Solution

The base voltage is

$$V_B = V_{R_2} = \frac{R_2}{R_1 + R_2} \times V_{cc}$$

Here, $R_2 = 5\ \text{k}\,\Omega = 5 \times 10^3\ \Omega$; $R_1 = 40\ \text{k}\,\Omega = 40 \times 10^3\ \Omega$; $V_{cc} = 12\ \text{V}$.

Therefore,

$$V_2 = \frac{5 \times 10^3}{(40 + 5) \times 10^3} \times 12 = 1.3\ \text{V}$$

The emitter voltage

$$V_E = V_2 - V_{BE} = 1.3 - 0.3 = 1.0\ \text{V}$$

Therefore, the emitter current

$$I_E = \frac{V_E}{R_E} = \frac{1.0}{1 \times 10^3} = 1.0 \times 10^{-3}\text{A}$$

The collector current,

$$I_C + I_E = 1.0\ \text{mA}$$

The collector voltage

$$V_C = V_{CC} - I_C R_C$$

$$= 12 - 1 \times 10^{-3} \times 5 \times 10^3 = 7\text{V}$$

Finally, the collector-to-emitter voltage

$$V_{CE} = V_C - V_E = 7 - 1 = 6\text{V}$$

Try to solve the following SAQ

SAQ 1

Suppose you have built a circuit as in Fig.4.11c. Predict what will happen in the following case : If R_1 is increased by 50% then

(a) V_{R_2} will..... b) V_{RE} will.....

(c) I_C will..... d) V_C will.....

4.5 SMALL SIGNAL AMPLIFIER

In the last section we discussed ways to bias a transistor for linear operation. After the transistor has been biased with a Q Point near the middle of the dc load line we can couple a small ac signal into the transistor. This produces fluctuations in the collector current of the same frequency and shape. For example, if the input is a sine wave with a frequency of 1 kHz, the output will be an enlarged sine wave with a frequency of 1 kHz. The amplifier is called a linear amplifier if it does not change the shape of the signal . As long as the amplitude of the input signal is small, the transistor will use only a small portion of the load line and the operation will be linear.

Look at the output characteristics of a transistor shown in Fig.4.12. The operating point Q is defined by I_{CQ}, V_{CEQ} & I_{BQ}.

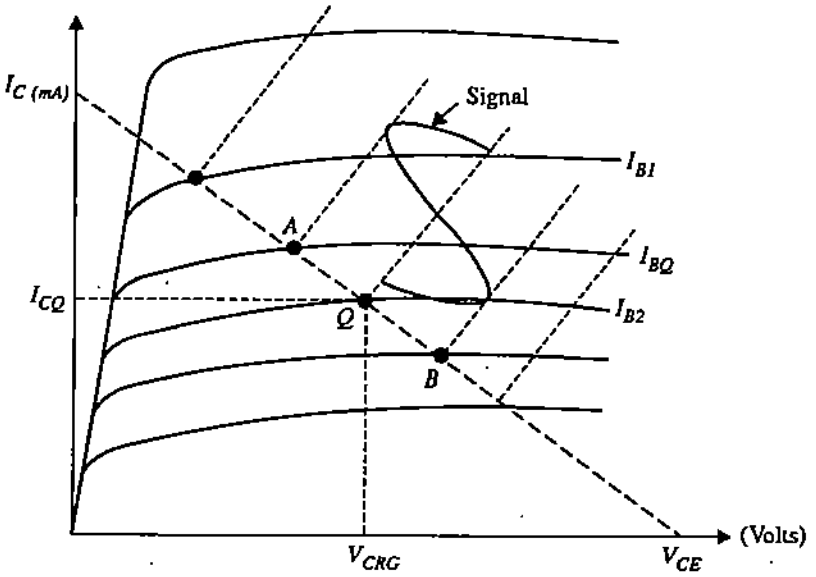


Fig. 4.12 : Swing of Q-point for a sinusoidal input.

When a sinusoidal signal is applied to the base, the base current changes to I_{B_1} during positive half cycle of the signal and to I_{B_2} during the negative half. The Q-point swings from Q to A and Q to B during this time. You can observe that under all circumstances the operating point remains on the linear portion of the characteristics. So an amplifier in which the operation is linear for the applied signal, is called a small signal amplifier.

This section introduces some ideas needed to analyze small signal amplifier. We will begin with coupling capacitors, devices that allow us to couple ac signals into and out of a transistor stage without changing the dc bias voltages.

4.5.1 Coupling and Bypass Capacitors

A coupling capacitor passes an ac signal from one point to another. In Fig.4.13(a) the ac voltage at point A is transmitted to point B. For this to happen, the capacitive reactance X_C must be very small compared with the series resistances. A bypass capacitor is similar to a coupling capacitor, except that it couples an ungrounded point to a grounded point, as shown in Fig.4.13(b).

In Fig.4.13(c), the capacitor ideally looks like a short to an ac signal. Because of this, point A is shorted to ground as far as the signal is concerned. This is why we have labelled point A as ac ground. A bypass capacitor will not disturb the dc voltage at point A because it looks open to dc current. However, a bypass capacitor makes point A an ac ground point.

4.5.2 Multi-Stage Amplifiers

An amplifier is the basic building block of most electronic systems. Just as one brick does not make a house, a single-stage amplifier is not sufficient to build a practical electronic system. In section 4.3, we had discussed the single-stage amplifier. The gain of single

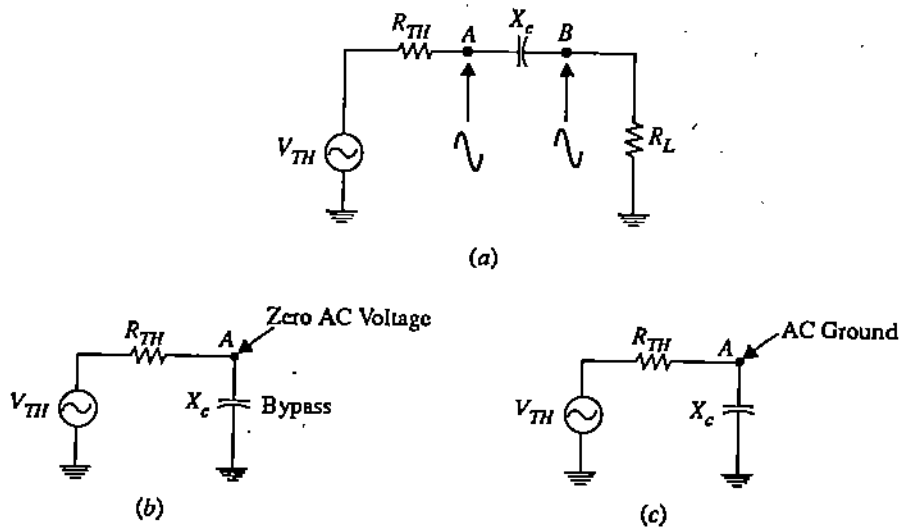


Fig. 4.13: a) Coupling capacitor between source and load.
b) Bypass capacitor
c) Bypass capacitor.

stage is not sufficient for practical applications. The voltage level of a signal can be raised to the desired level if we use more than one stage. When a number of amplifier stages are used in succession (one after the other) it is called a multi-stage amplifier or a cascaded amplifier. Much higher gains can be obtained from the multi-stage amplifier.

Gain of a Multi Stage Amplifier

A multi-stage amplifier (n-stages) can be represented by the block diagram as shown in Fig.4.14. You may note that the output of the first stage makes the input of the second

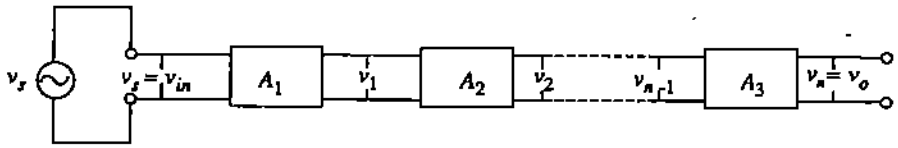


Fig. 4.14: Block diagram of a multistage amplifier having n stages.

stage: the output of the second stage makes the input of the third stage,....., and so on. The signal voltage v_s is applied to the input of the first stage. The final output v_o is then available at the output terminals of the last stage. The output of the first (or the input to the second stage) is

$$v_1 = A_1 v_s$$

where A_1 is the voltage gain of the first stage. Then the output of the second stage (or the input to the third stage) is

$$v_2 = A_2 v_1$$

Similarly, the final output v_o is given as

$$v_o = v_n = A_n v_{n-1}$$

where A_n is the voltage gain of the last (nth) stage.

We may look upon this multi-stage amplifier as a single amplifier, whose input is v_s and output is v_o. The overall gain A of the amplifier is then given as

$$A = \frac{v_o}{v_s} = \frac{v_1}{v_s} \times \frac{v_2}{v_1} \times \ldots \times \frac{v_{n-1}}{v_{n-2}} \times \frac{v_o}{v_{n-1}}$$

or

$$A = A_1 \times A_2 \times \ldots \times A_{n-1} \times A_n \tag{4.23}$$

The gain of an amplifier can also be expressed in another unit called **decibel**.

Decibel

In many problems it is found very convenient to compare two powers on a logarithmic scale rather than on a linear scale. The number of bels by which a power P_2 exceeds a power P_1 is defined as

$$\text{Number of bels} = \log_{10} \frac{P_2}{P_1}$$

For practical purposes it has been found that the unit bel is quite large. Another unit, one-tenth as large, is more convenient. This smaller unit is called the decibel (abbreviated as dB), and since one decibel is one-tenth of a bel, we have

$$\text{Number of dB} = 10 \times \text{Number of bels} = 10 \log_{10} \frac{P_2}{P_1} \tag{4.24}$$

For an amplifier, let P_1 represents the input power and P_2 the output power: If V_1 and V_2 are the input and output voltages of the amplifier, then

$$P_1 = \frac{V_2^1}{R_1}$$

and

$$P_2 = \frac{V_2^2}{R_o}$$

Where, R_I and R_o are the input and output impedances of the amplifier. Then, Eq.(4.24) can be written as

$$\text{Number of dB} = 10 \log_{10} \frac{V_2^2/R_o}{V_2^1/R_I}$$

In case the input and output impedances of the amplifier are equal , i.e. $R_I = R_o = R$, the Eq.(4.24) simplifies to

$$\text{Number of dB} = 10 \log_{10} \frac{V_2^2}{V_2^1} = 10 \log_{10} \left\{\frac{V_2}{V_1}\right\}^2 \tag{4.25}$$

$$= 10 \times 2 \log_{10} \frac{V_2}{V_1} = 20 \log_{10} \frac{V_2}{V_1}$$

However, in general, the input and output impedances are not always equal. But the expression of Eq.(4.25) is adopted as a convenient definition of the decible voltage gain of an amplifier, regardless of the magnitudes of the input and output impedances.

As an example: if the voltage gain of an amplifier is 10, it can be denoted on the dB scale as

$$\text{Gain in dB} = 20 \log_{10} \frac{V_2}{V_1} = 20 \log_{10} 10$$

$$= 20 \times 1 = 20 \text{ dB}$$

Gain of Multi-Stage Amplifier in dB

The gain of a multi-stage amplifier can be easily computed if the gains of the individual stages are known in dB. The overall voltage gain in dB of a multi-stage amplifier is the sum of the decibel voltage gains of the individual stages. That is

$$A_{dB} = A_{dB1} + A_{dB2} + \ldots + A_{dBn} \tag{4.76}$$

SAQ 2

A multi-stage amplifier consists of three stages. The voltage gains of the stages are 30, 50 and 80. Calculate the overall voltage gain in dB. Also calculate the overall gain using Eq.4.23.

How to Couple Two Stages

In a multi-stage amplifier, the output of one stage makes the input of the next stage (see Fig.4.14). Can we connect the output terminals of one amplifier to the input terminals of the next amplifier directly ? This may not always be possible due to practical difficulties. We must use a suitable coupling network between two stages so that a minimum loss of voltage occurs when the signal passes through this network to the next stage. Also, the dc voltage at the output of one stage should not be permitted to go to the input of the next. If it does, the biasing conditions of the next stages are disturbed.

The coupling network not only couples two stages; it also forms a part of the load impedance of the preceding stage. Thus, the performance of the amplifier will also depend upon the type of coupling network used. The three generally used coupling schemes are :

(i) Resistance-capacitance coupling

(ii) Transformer coupling

(iii) Direct coupling

Resistance-Capacitance Coupling

Fig.4.15 shows how to couple two stages of amplifiers using resistance-capacitance (RC) coupling scheme. This is the most widely used method. In this scheme, the signal developed across the collector resistor R_c of the first stage is coupled to the base of the second stage through the capacitor C_c. The coupling capacitor C_c blocks the dc voltage of the first stage from reaching the base of the second stage. In this way, the dc biasing of the next stage is not interfered with. For this reason, the capacitorC_c is also called a blocking capacitor.

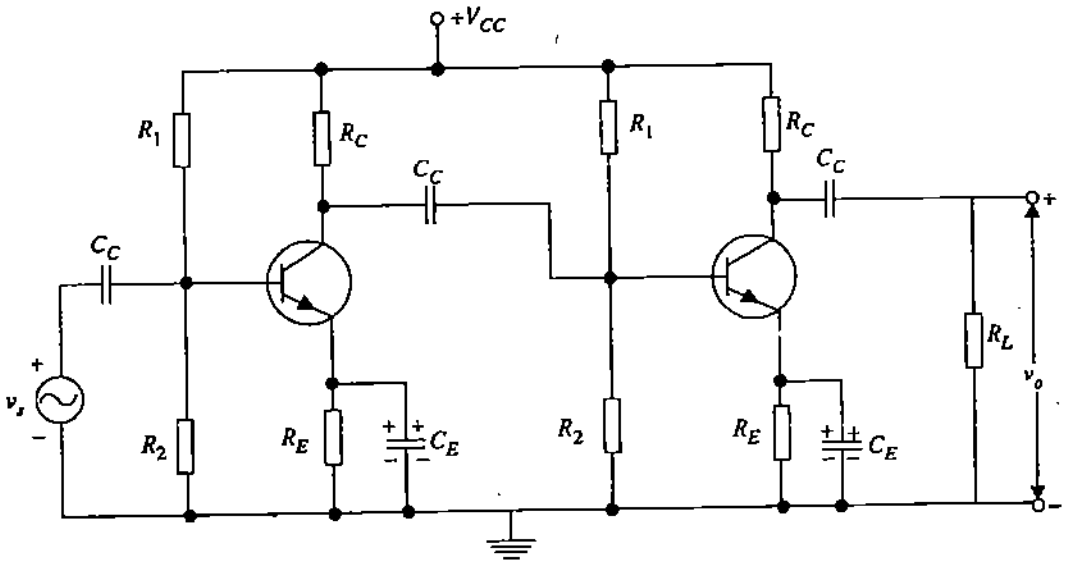


Fig. 4.15 : Two-stage *RC*-coupled amplifier using transistors.

Transformer Coupling

In this type of coupling, a transformer is used to transfer the ac output voltage of the first stage to the input of the second stage. The resistor R_c (see Fig.4.15) is replaced by the primary winding of the transformer. The secondary winding of the transformer replaces the wire between the voltage divider (of the biasing network) and the base of the second stage. Fig.4.16 illustrates the transformer coupling between the two stages of amplifiers.

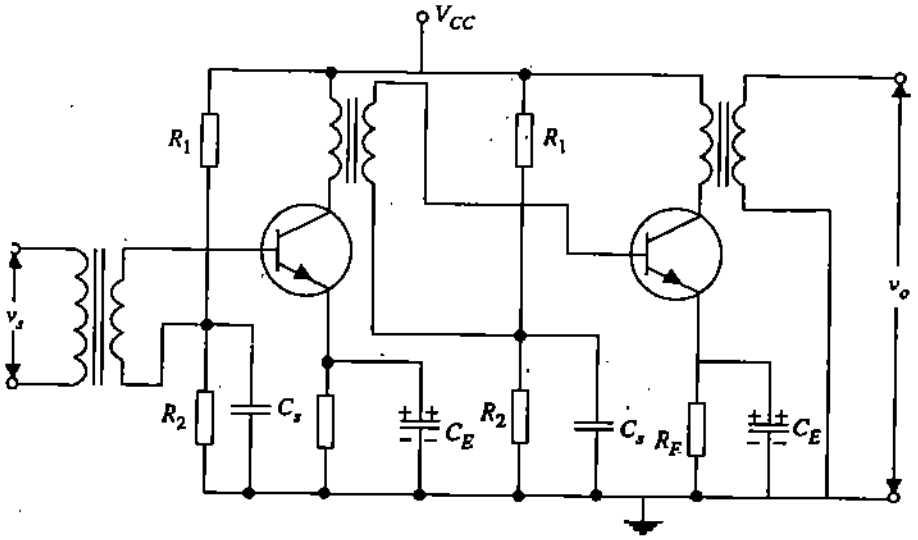


Fig. 4.16: Two stages, using transistors, are coupled by a transformer.

Note that in this circuit there is no coupling capacitor. The dc isolation between the two stages is provided by the transformer itself. There exists no dc path between the primary and the secondary windings of a transformer. However, the ac voltage across the primary winding is transferred (with a multiplication factor depending upon the turns ratio of the transformer) to the secondary winding.

The main advantage of the transformer coupling over *RC* coupling is that all the dc voltage supplied by V_{cc} is available at the collector. There is no voltage drop across the collector resistor R_c (of *RC*-coupled). The absence of resistor R_c in the collector circuit also eliminates the unnecessary power loss in the resistor.

The transformer coupling scheme is not used for amplifying low frequency (audio) signals. However, they are widely used for amplification of radio-frequency signals(above 20 kHz). In radio receivers, the rf ranges from 550 kHz to 1600 kHz for the medium-wave band: and from 3 MHz to 30 MHz for the short wave band. In TV receivers, the rf signals have frequencies ranging from 54 MHz to 216 MHz. By putting suitable shunting capacitors across each winding of the transformer, we can get resonance at any desired rf frequency. Such amplifiers are called tuned-voltage amplifiers. These provide high gain at the desired rf frequency. For this reason, the transformer-coupled amplifiers are used in radio and TV receivers for amplifying rf signals, (such amplifiers are discussed in section 4.7).

The use of a transformer for coupling also helps in proper impedance matching. By suitably selecting the turns ratio of the transformer, we can match any load with the output impedance of the amplifier. This help in transferring maximum power from the amplifier to the load. This is discussed in more details in section 4.6 on power amplifier.

Direct Coupling

In certain applications, the signal voltages are of very low frequency. The amplifier used for the amplification of such slowly varying signals makes use of direct coupling. In this type of coupling scheme, the output of one stage of the amplifier is connected to the input of the next stage by means of a simple connecting wire.

For applications where the signal frequency is below 10 Hz, coupling capacitors and bypass capacitors cannot be used. At low frequencies, these capacitors can no longer be treated as short circuits, since they offer sufficiently high impedance. Fig.4.17 shows a two stage direct coupled amplifier.

The direct coupling scheme has a serious drawback. The transistor parameters like V_{BE} and β vary with temperature. This causes the collector current and voltage to change. Because of the direct coupling, this voltage change appears at the final output.

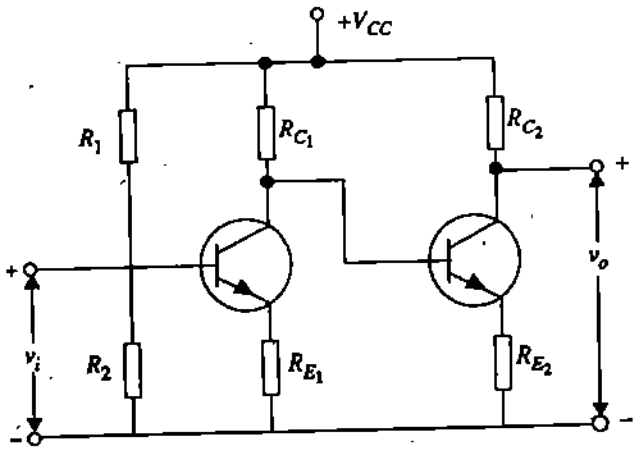


Fig. 4.17: Two stage, direct-coupling amplifier using transistors.

4.5.3 Frequency Response of an *RC*-Coupled Amplifier

A practical amplifier circuit is meant to raise the voltage level of the input signal. This signal may be obtained from the sound head of a tape recorder, the microphone in case of a PA system. Such a signal is not of a single frequency. But it consists of a band of frequencies. For example, the electrical signal produced by the voice of human being or by a musical orchestra may contain frequencies as low as 30 Hz and as high as 15 kHz. If the loudspeakers are to reproduce the original sound faithfully, the amplifier used must amplify all the frequency components of the signal equally well. If it does not do so, the output of the loudspeaker will not be an exact replica of the original sound.

The performance of an amplifier is judged by observing whether all frequency components of the signal are amplified equally well. This information is provided by its frequency response curve. This curve illustrates how the magnitude of the voltage gain of amplifier varies with the frequency of the input signal (simusoidal).

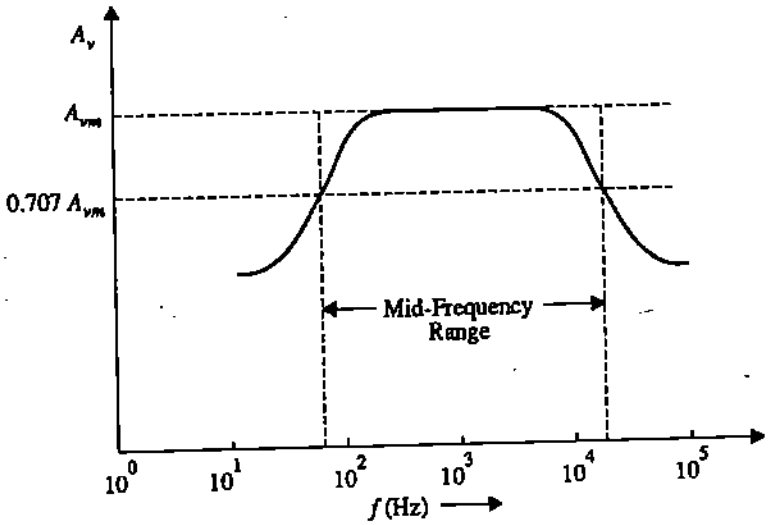


Fig.4.18: Frequency response curve of an *RC*-coupled amplifier.

Fig.4.18 shows a frequency response curve of a typical *RC*-coupled amplifier. Note that the gain is constant only for a limited band of frequencies. This range of frequencies is called the mid-frequency range and the gain is called mid-band gain, A_m. On both sides of the mid-frequency range, the gain decreases. For very low and for very high frequencies, the gain of the amplifier reduces to almost zero.

Low-frequency Range

In the section 4.3, we analysed an amplifier circuit to determine its voltage gain. This was the mid-frequency gain. In mid-frequency range, the coupling and bypass capacitors are as good as short circuits. But, when the frequency is low, these capacitors can no longer be replaced by the short circuit approximation. The lower the frequency, the greater is the value of reactance of these capacitors, since

$$X_c = \frac{1}{2\pi fC}$$

This causes a significant voltage drop across C_c. The result is that the effective output voltage decreases. The lower the frequency of this signal, higher will be the reactance of the capacitor C_c and more will be the reduction in output voltage. At zero frequency (dc signals), the reactance of capacitor C_c is infinitely large (an open circuit). The effective output voltage then reduces to zero. Thus we see that the output voltage (and hence the voltage gain) decreases as the frequency of the signal decreases below the mid-frequency range.

The other component, due to which the gain decreases at low frequencies is the bypass capacitor C_E. The coupling capacitor in the input side is also responsible for the decrease of gain at low frequencies.

In practical circuits, the value of the bypass capacitor C_E is very large (=100 μF). Therefore, it is the coupling capacitor that has the more pronounced effect in reducing the gain at low frequencies.

High Frequency Range

As the frequency of the input signal increases, the gain of the amplifier reduces. Several factors are responsible for this reduction in gain . Firstly, the beta (β) of the transistor is frequency dependent. Its value decreases at high frequencies. Because of this, the voltage gain of the amplifier reduces as the frequency increases.

Another important factor responsible for the reduction in gain of the amplifier at high frequencies is the presence of the device. In case of a transistor, there exists some capacitance due to the formation of a depletion layer at the junctions. These inter-electrode capacitances C_{bc}, C_{be}, C_{ce} are shown in Fig.4.19. Note that the connection for these capacitances are shown by dotted lines to indicate that these are not physically present in the circuits, but are inherently present with the device (whether we like it or not).

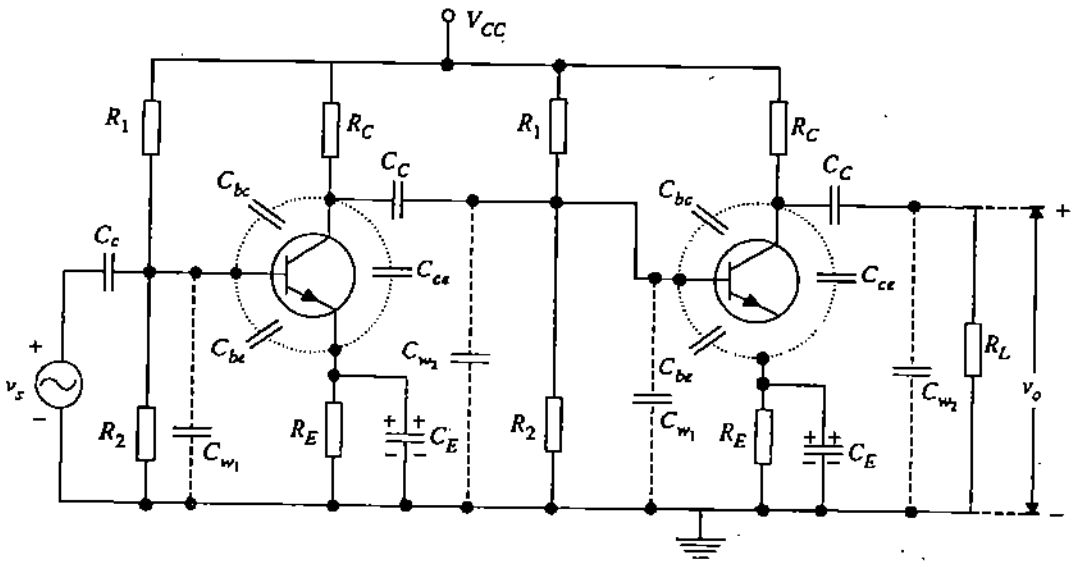


Fig.4.19: *RC*-coupled amplifier. Capacitances that affect high-frequency response are shown by dotted connections.

Besides the junction capacitances, there are wiring capacitances C_{w1} and C_{w2} as shown in Fig.4.19. The effect of the capacitance C_{ce}, C_{w2} and the input capacitance C_i of the next stage can be represented by a single shunt capacitance. At high frequency these capacitance become

$$C_s = C_{ce} + C_{w2} + C_i$$

Note that at high frequency, the impedence offered by the coupling capacitor is negligible.

As the frequency of the input signal increases, the impedance of the shunt capacitance C_3 decreases, since

$$X_{cs} = \frac{1}{2\pi f C_s}.$$

The higher the frequency, the lower is the impedance offered by C_3 and lower will be the output voltage.

Bandwidth of an Amplifier

Frequency response curve of an *RC*-coupled amplifier of Fig.4.18, shows that the gain remains constant only for a limited band of frequencies. On both the low-frequency side as well as on the high frequency side, the gain falls. Now, an important question arises-where exactly should we fix the frequency limits (of input signal) within which the amplifier may be called a good amplifier ? The limit is set at those frequencies at which the voltage gain reduces to 70.7% of the maximum gain A_m. These frequencies are known as the cut-off frequencies of the amplifier. These frequencies are marked in Fig.4.18. The frequency f_1 is the lower cut off frequency and the frequency f_2 is the upper cut-off frequency. The difference of the two frequencies, that is $f_2 - f_1$, is called the bandwidth (*BW*) of the amplifier. The mid-frequency range of the amplifier is from f_1 to f_2. Usually, the lower cut-off frequency f_1 is much lower than the upper cut-off frequency f_2, so that we have

$$BW = f_2 - f_1 = f_2 .$$

Example 2

An *RC*-coupled amplifier has a voltage gain of 100 in the frequency range of 400 Hz to 25 kHz. On either side of these frequencies, the gain falls so that it is reduced by 3 dB at 80 Hz and 40 kHz. Calculate gain in dB at cut-off frequencies and also construct a plot of frequency response curve.

Solution

The gain in dB is

$$A_{dB} = 20 \log_{10} A = 20 \log_{10} 100 = 40 \text{ dB}$$

This is the mid band gain. The gain at cut-off frequencies is 3 dB less than the mid band gain, i.e.

$$(A_{dB}) \text{ (at cut-off frequencies)} = 40 - 3 = 37 \text{ dB}$$

The plot of the frequency response curve is given in Fig.4.20.

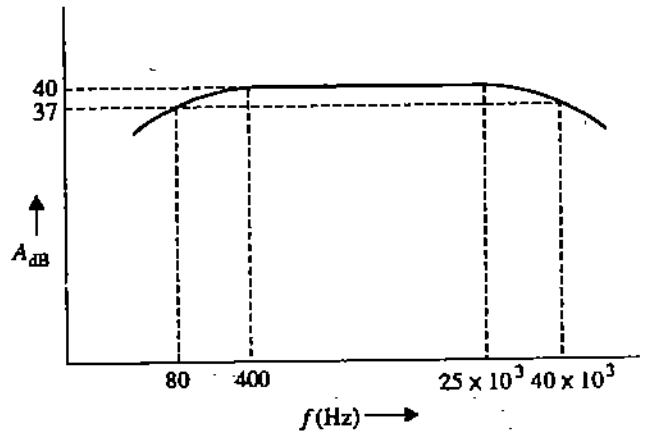


Fig. 4.20: *RC*-coupled amplifier Capacitances that affect high-frequency response are shown by dotted connections.

4.6 LARGE SIGNAL AMPLIFIERS

In almost all electronic systems, the last stage has to be a power amplifier. For example, in a public address system, it is the power amplifier that drives the loudspeakers. When a person speaks into a microphone, the sound waves are converted by it into electrical signal.

This electrical signal is of very low voltage (a few mV). This signal, if fed directly, cannot drive the loudspeakers, to give sound (audio) output. The voltage level of this signal is first raised to sufficiently high values (a few V) by passing it through a multi-stage voltage amplifier. This voltage is then used to drive (or excite) the power amplifier. The power amplifier is capable of delivering power to the loudspeakers. The loudspeakers finally convert the electrical energy into sound energy. Thus, a large audience can hear the speech (or music from the orchestra, tape recorder, record player, or any other such gadget).

Thus we find that a power amplifier is an essential part of every electronic system.

The primary function of the voltage amplifier is to raise the voltage level of the signal. It is designed to achieve the largest possible voltage gain. Only very little power can be drawn from its output. On the other hand, a power amplifier is meant to boost the power level of the input signal. This amplifier can feed a large amount of power to the load. To obtain large power at the output of the power amplifier, its input-signal voltage must be large. That is why, in an electronic system, a voltage amplifier precedes the power amplifier. Also, that is why the power amplifiers are called large-signal amplifiers.

Now the question arises that why a voltage amplifier cannot work as a power amplifier or in other words what is the difference between a voltage amplifier and a power amplifier. Refer to Fig.4.15 of section 4.5.

The total dc power drawn from the supply is $V_{CC}\ I_{CQ}$. Out of this, only $V_{CEQ}\ I_{CQ}$ is the effective dc input power to the amplifier because, at best, that is the power that could be converted into useful ac power. The difference of power which is

$$I_{co}^2\,(R_C + R_E)$$

goes waste in unnecessarily heating the resistors.

We can attempt to reduce this wastage of power. The resistor R_E has to be there in the circuit, because it is a part of the biasing network. If R_E is absent, the stabilisation of the operating point becomes poor. However, we can do something about the resistance R_C.

We can replace R_C by a component whose dc resistance is zero, but ac impedance is very high. We can do this by replacing R_C by a choke (an inductor). Two things are achieved by doing this. First, no dc voltage drop occurs across the choke (since the dc resistance is almost zero). We can afford to use lower voltage supply V_c for the same amplifier. Second, the dc power loss in the choke is almost nil. Thus, this circuit is much better as compared to the one in Fig.4.15.

Still more improvements can be made in this circuit so that it works as a better power amplifier. How it happens is explained in the next subsection.

4.6.1 Single-ended Power Amplifier

Fig.4.21 shows a typical single ended transistor power amplifier. The term "single-ended" (denoting only one transistor) is used to distinguish this type from the push-pull amplifier (which uses two transistors; and is discussed in next subsection).

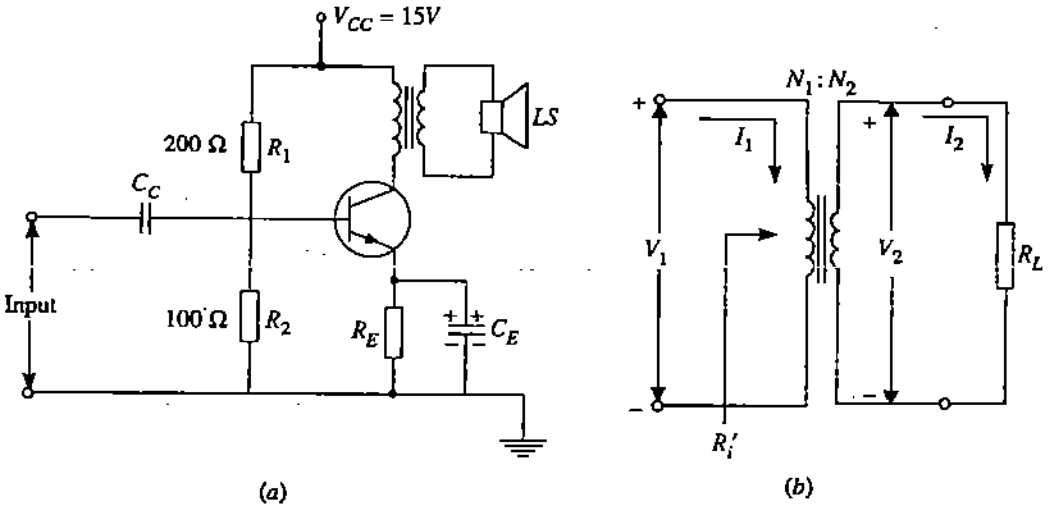


Fig.4.21: Single ended power amplifier.

In many electronic systems, such as radio, television, tape recorder, public address system, etc. the final output is in the form of sound. In such systems, the loudspeaker is the load for the power amplifier. The power amplifier makes the final stage and it drives the loudspeaker. In place of choke we have used a transformer in the circuit because it provides impedence matching.

In a power amplifier, the ac output power is sufficiently high, whereas the power in the base circuit is quite low. The question naturally arises where the power comes from. The only source of power in a power amplifier is the dc supply, V_{CC}. A portion of this dc input power appears as useful ac power across the load R_L. The rest of it is lost in the circuit. That is

dc input power =ac output power + losses

or

$$P_i \text{ (dc)} = P_o \text{ (ac)} + \text{Losses} \tag{4.27}$$

In Eq. (4.27), the input dc power is obtained from the battery. It is given by the product of voltage V_{CC} and the average current drawn from the battery. If the amplifier is working in class-A operation, the average collector current will be the same as the quiescent collector current I_{CQ}. Therefore, the dc input power is

$$P_i = V_{CC} I_{CQ} \tag{4.28}$$

For the transformer coupled amplifier, the only power lost is P_D which is dissipated by the transistor (other losses are negligible). We can now write Eq. 4.27 as

$$P_D = P_i + P_o$$

or

$$P_D = V_{CC} I_{CQ} + P_o \tag{4.29}$$

This equation is very significant in the operation of a power amplifier. The maximum power dissipation in the transistor occurs when the ac output power is zero, in which case

$$P_{D\,(max)} = V_{CC} I_{CQ} \tag{4.30}$$

Fig.4.22 shows collector characteristics of a power transistor. Assume that its dissipation rating is 3.5 W, we must ensure P_D does not exceed 3.5 W. We first plot its collector dissipation curve. We take some arbitrary values of V_{CE} and calculate corresponding values of I_C so that we always have $V_{CE} I_C = P_D = 3.5$W. The curve obtained from these values is a hyperbola, as shown in Fig.4.22. If this transistor is used in a power amplifier, its Q point must lie below this curve.

A power amplifier is said to have high efficiency, if it can convert a greater portion of the dc input power drawn from the battery into the useful ac output power. We define output-circuit efficiency as the ratio of ac power to dc input power supplied to the collector-emitter circuit.

$$\eta = \frac{P_o \text{ (ac)}}{P_i \text{ (dc)}} = \frac{P_o}{V_{CC}\ I_{CQ}} \tag{4.31}$$

Efficiency is a measure of how well an amplifier converts dc power from the battery into useful ac output power.

Let us analyse the circuit shown in Fig.4.23. The collector characteristics of the transistor are given in Fig.4.22. We shall find, for this circuit, the rms values of collector current and voltage, and the ac power developed at the collector and the collector-circuit efficiency

To analyse the circuit, we first draw the dc load line on the collector characteristics. The dc resistance of the primary of the transformer is assumed to be 0 Ω. Also, the resistance R_E is negligibly small. The dc load line is therefore a vertical straight line.

From the graph in Fig.4.22, we can find the maximum and minimum values of the collector current and voltage, between which the signal swings. The ac power developed across the transformer primary can be calculated to be

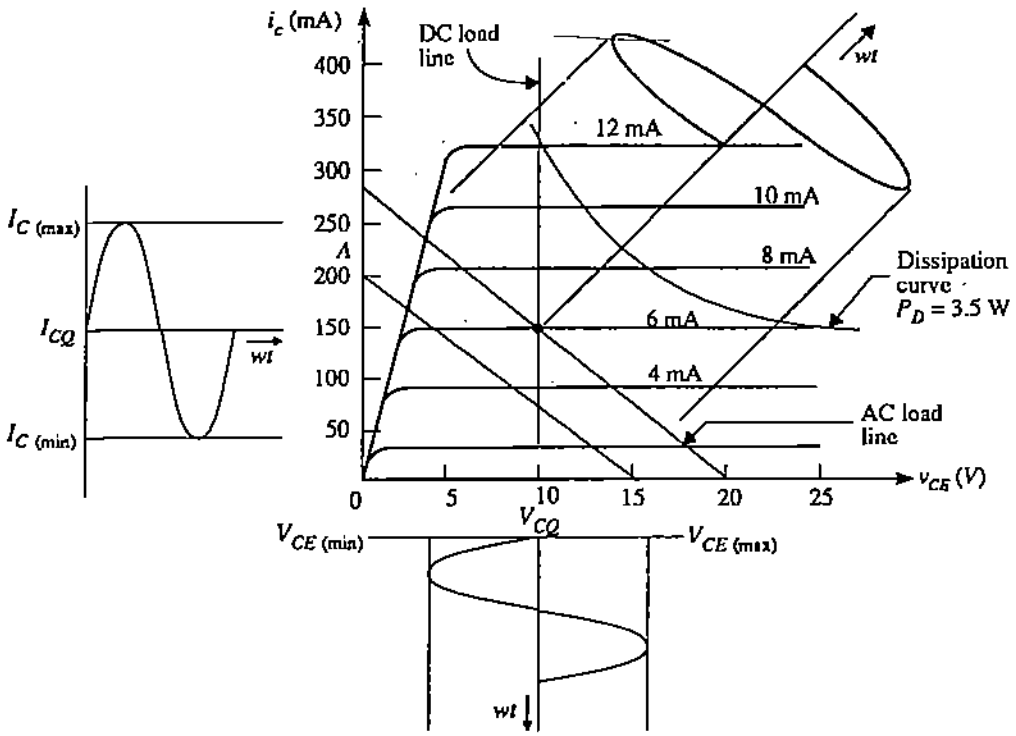


Fig.4.22: Characteristics of a power transistor with its collector dissipation curve.

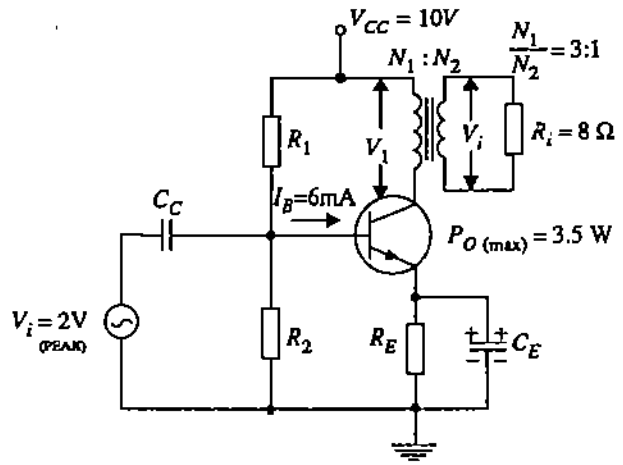


Fig. 4.23: A practical single-ended amplifier.

$$P_o\,(\text{ac}) = V_{CE}\,(\text{rms}) \times I_C\,(\text{rms}) = \frac{V_{CC}\,(\text{peak})}{\sqrt{2}} \times \frac{I_c\,(\text{peak})}{\sqrt{2}}$$

$$= \frac{(V_{CE\,(max)} - V_{CE\,(min)})}{2\sqrt{2}} \; \frac{(I_{C\,(max)} - I_{C\,(min)})}{2\sqrt{2}} \qquad (4.32)$$

or

$$P_o = \frac{[(V_{CE\,(max)} - V_{CE\,(min)}]\;[(I_{C\,(max)} - I_{C\,(min)}]}{8}$$

The same power appears across the load R_L, if the transformer is 100% efficient. Assuming the losses in the transformer to be negligible, we may now calculate the ac power delivered to the loudspeaker R_L from Eq. 4.32.

In this case,

transistors flow in opposite directions through the two halves of the primary winding. These currents produce opposite flux through the magnetic core of the transformer. If the two transistors are perfectly matched, the net flux in the core is zero.

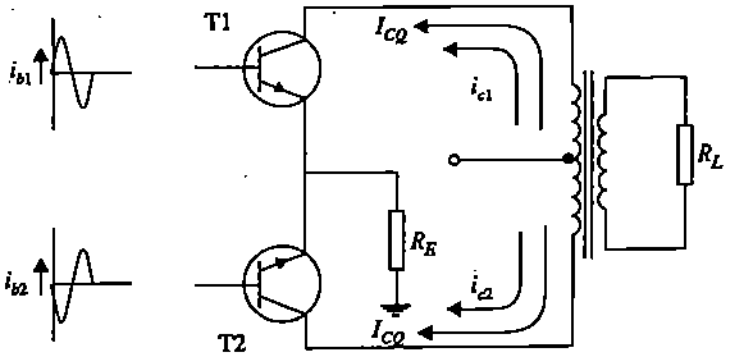


Fig.4.26: Details of push-pull operation at the output.

When an ac signal is applied to the input, opposite phased, varying base currents flow in the two transistors. As a result, the ac collector currents in the two transistors are also in opposite phase. The total current i_{c1} in transistor T_1 and the total current i_{c2} in transistor T_2 varies as shown in Fig.4.27a and b, respectively. These currents flow in opposite directions in two halves of the primary winding. The flux produced by these currents will also be in opposite directions. The net flux in the core will be the same as that produced by the difference of the currents i_{c1} and i_{c2}. To find the difference i_{c1} and i_{c2}, we first find the negative of i_{c2}. This is done in Fig.4.27c. We can now add the currents of Fig.4.27a and to get the difference, since

$$i_{c1} - i_{c2} = i_{c1} + (-i_{c2})$$

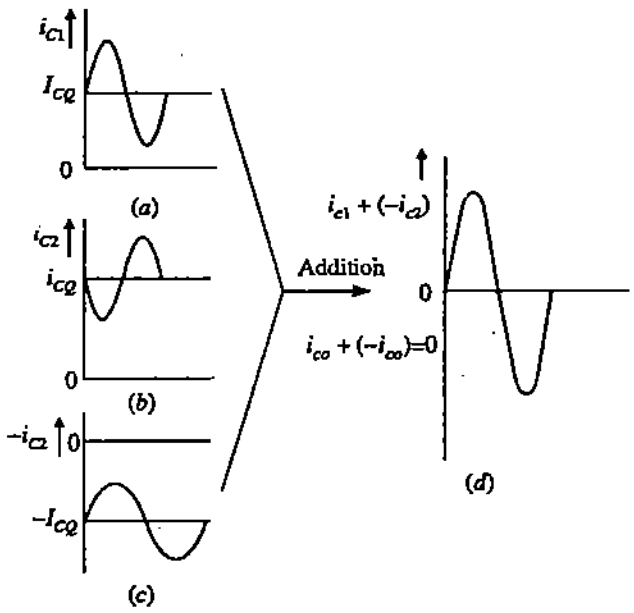


Fig. 4.27: (a) Collector current i_{c_1} in transister T_1
(b) Collector current i_{c_2} in transistor T_2
(c). The negative of i_{c_2}
(d) The difference $i_{c_1} - i_{c_2}$.

The difference of the two collector currents is obtained in Fig.4.27d. Note that during this process the quiescent currents (I_{CQ}) of the two transistors get cancelled, but the ac currents get added up. The overall operation results in a net ac current flow through the primary of the transformer. This results in a varying flux in the core. An ac voltage is induced in the secondary, and the ac power is delivered to the load resistor R_L.

From Fig. 4.27a and b, it may be seen that during the first half-cycle, the current i_{c1} increases, but at the same time the current i_{c2} decreases. In other words, when one

transistor is being driven into more conduction, the other is driven into less conduction. The reverse happens in the next half-cycle. This amounts to saying that when the current in one transistor is "pushed up", the current in the other transistor is "pulled down". Hence, the name push-pull amplifier.

4.7 RADIO FREQUENCY (rf) AMPLIFIERS

Till now we have discussed audio amplifiers. Such amplifiers are used in various audio systems, for example, record players, tape recorders, public address systems etc. In radio broadcasting, the audio signal (voice or music) is "raised" to some high-frequency level. This high frequency is in the radio-frequency (rf) range and it serves as the carrier of the audio signal. The carrier frequencies (and corresponding wavelengths) of some of the broadcast stations are given below:

Station	Frequency	Wavelength
Delhi 'B'	1017 kHz	294.9 m
Bombay 'C'	1188 kHz	252.5 m

The process of raising the audio signal to rf frequencies is called modulation. It is the modulated wave that is transmitted by the broadcasting station. This modulated wave has a relatively narrow band of frequencies centred around the carrier frequency, as shown in Fig.4.28. The bandwidth of the signal $f_2 - f_1$ is very small compared to the carrier frequency f_c.

When the rf signal (modulated wave) reaches the receiving antenna, a very weak voltage is induced in it. This voltage is of the order of a few μV. It is not possible to extract the original audio signal from this weak voltage. It is necessary, first, to amplify the rf signal to a suitable level. This is achieved in a radio receiver with the help of a tuned voltage amplifier also called radio frequency amplifier.

The process of extracting the original signal from the rf signals is called demodulation. These terms (modulation and demodulation are presented here merely by way of introduction. They will be discussed in detail when we deal with communication.

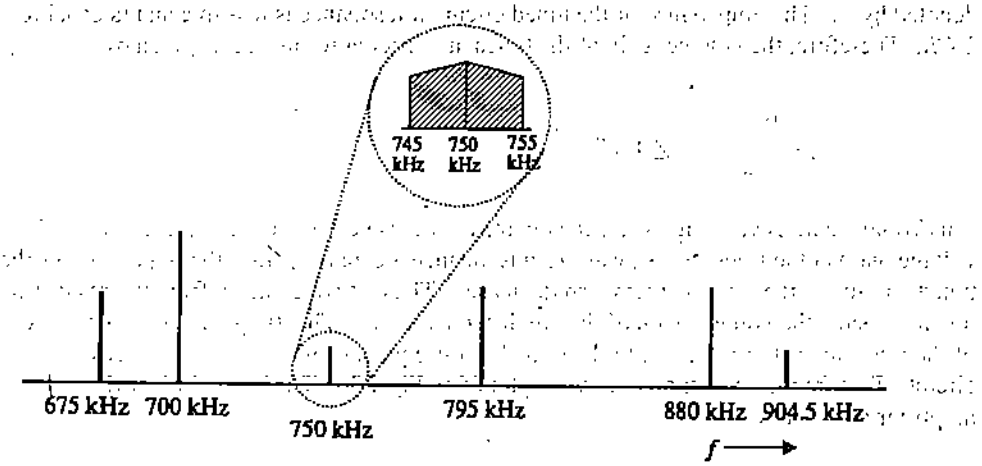


Fig. 4.28: Frequency spectrum of modulated waves that are transmitted by different broadcasting stations.

A tuned-voltage amplifier uses a tuned circuit. The radio frequency amplifier can be classified into two: single tuned voltage amplifier and double tuned voltage amplifier.

4.7.1 Single-tuned Voltage Amplifier

Fig.4.29 shows the circuits of a single-tuned voltage amplifier. In the circuit of Fig.4.29a, the output is taken with the help of capacitive coupling, whereas in Fig.4.29b, the output is obtained by inductive coupling.

In Fig.4.29, the resistors R_1 and R_2 and R_E fix up the operating point and also stabilize it. The tuned circuit consisting of inductance and capacitance acts like a load resistance of amplifier circuit. One of the two components, that is, either inductance, or capacitance, is variable. This is for adjusting the resonant frequency of the circuit.

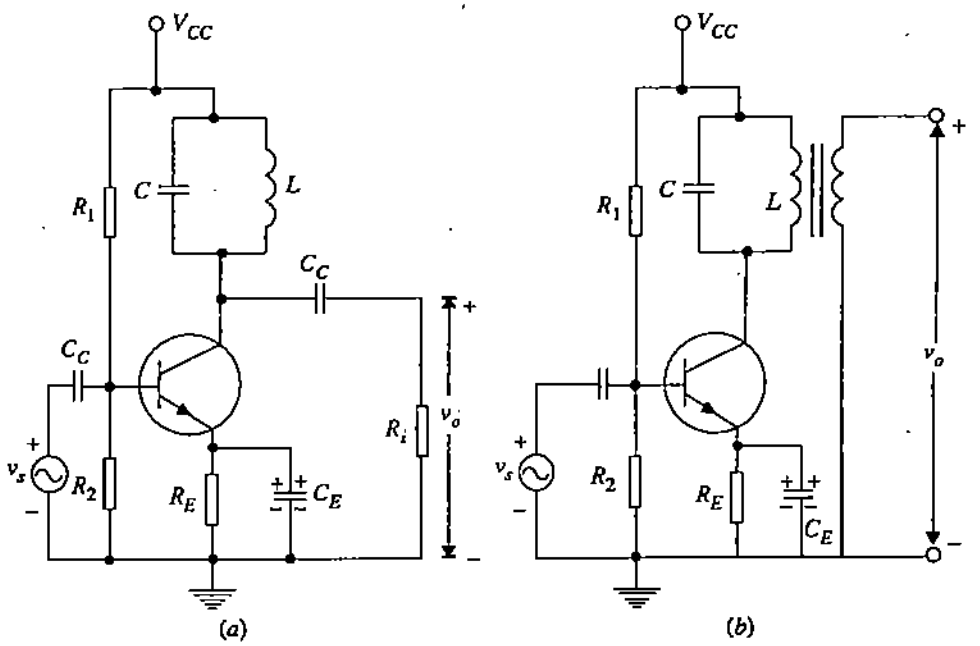


Fig.4.29: Single-tuned amplifier circuits using bipolar junction transistor :
a) Capacitively coupled amplifier.
b) Inductively coupled amplifier.

Voltage Gain and Frequency Response Curve

We have already studied that the voltage gain of an amplifier depends upon the ac load resistance.

$$A = \frac{\beta R_{ac}}{r_{in}} \quad \angle 180^\circ \quad \text{(where } 180^\circ \text{ shows that output)}$$

In the tuned amplifier, R_{ac} is the impedance of the tuned circuit. This impedance is denoted by Z_p. The impedance of the tuned circuit at resonance is resistive and is equal to L/CR. Therefore, the voltage gain of the tuned amplifier at resonance is given by

$$A = \frac{\beta \dfrac{L}{CR}}{r_{in}} \quad \angle 100^\circ$$

This voltage gain is very high since the quantity L/CR is very high for a tuned circuit. The voltage gain at the frequencies away from resonance decreases, since the impedance of the tuned circuit at these frequencies also decreases. Thus, as we go away from the resonance on either side, the voltage gain of the amplifier decreases. The frequency response curve of the tuned amplifier is similar to the impedance-frequency curve for a parallel resonant circuit. This frequency response curve is plotted in Fig.4.30. The bandwidth of the amplifier is given by

$$BW = \frac{f_r}{Q} \tag{4.35}$$

where, $$f_r = \frac{1}{2\pi\sqrt{LC}}. \tag{4.36}$$

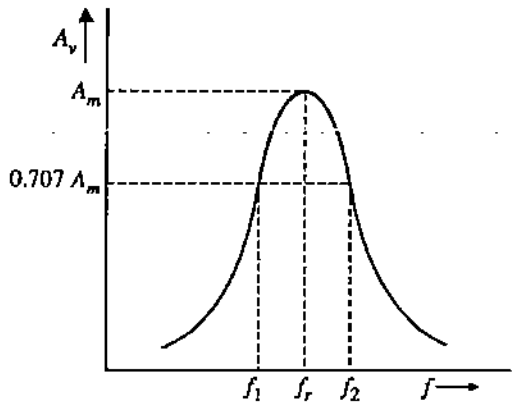


Fig.4.30: Frequency response curve of a single-tuned amplifier.

The above expression comes from the formula for bandwidth of a parallel resonant circuit.

Limitations of Single-tuned Voltage Amplifiers

Tuned voltage amplifiers are generally used in rf stage of wireless communication systems. Here, these circuits are assigned the work of selecting the desired carrier frequency and of amplifying the allowed pass band around this selected carrier frequency. The high selectivity requires a high Q-resonant circuit. A high Q circuit will have high gain too, but at the same time the bandwidth will be very much reduced. A very narrow band will result in poor reproduction. This is the drawback with a single-tuned circuit. However, this difficulty is overcome by using double-tuned circuit. In double-tuned amplifiers, there are two tuned circuits results in change in the shape of the frequency response curve. If the coupling between the two coils of the tuned circuits is properly adjusted, the required results (high selectivity, high gain and required bandwidth) may be obtained.

4.7.2 Double-Tuned Voltage Amplifier

In double-tuned circuits, inductive coupling is used. The primary and the secondary coils of the transformer are shunted by capacitors, thus making two tuned circuits. The circuit diagram of a double-tuned voltage amplifier is shown in Fig.4.31.

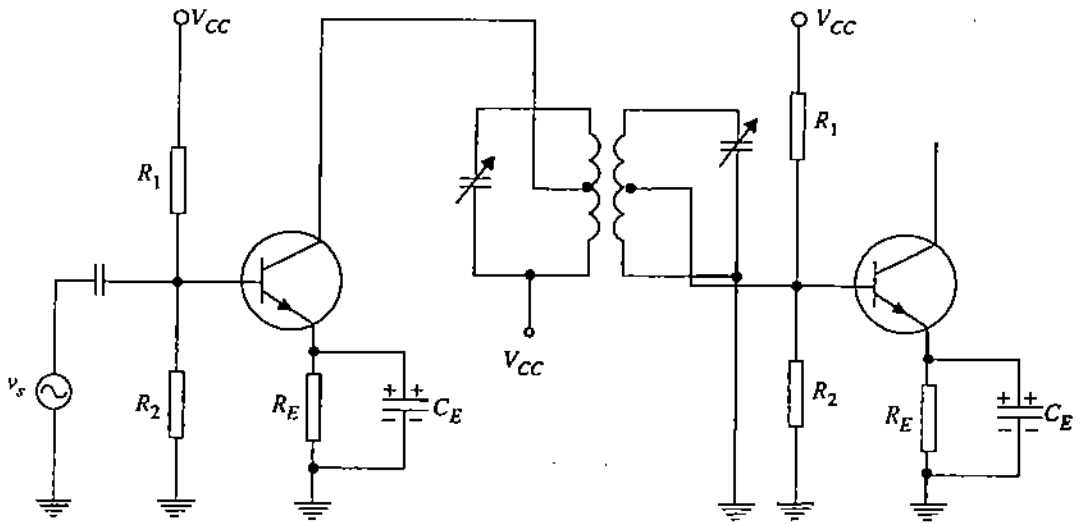


Fig.4.31: Double-tuned transistor amplifier.

The frequency response curve of the double-tuned amplifier for different coefficients of coupling is shown in Fig.4.32.

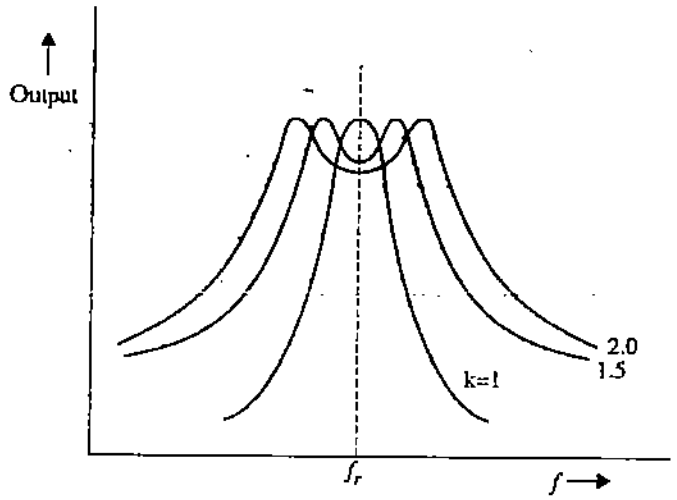


Fig.4.32: Frequency response curve of a double tuned amplifier for different coefficients of coupling.

It should be appreciated that the most suitable response curve is one when optimum coefficient of coupling exists between the two tuned circuits. In this condition, the circuit is highly selective and also provides sufficient amount of gain for a particular band of frequencies.

SAQ 3

A tuned amplifier consists of a parallel LC circuit, driven by a transistor with an output resistance of 100 kΩ?, and connected across a resistive load of 100 kΩ. The inductor has an inductance of 100 μH and the total equivalent capacitance (including stray capacitance) is 100 pF. Calculate the centre frequency, fr, and the bandwidth of the tuned amplifier.

1. Amplification is the process by which a signal's power is increased.
2. A transistor in CB or CE or CC configuration can be replaced by a *h*-parameter equivalent circuits.
3. The operating point (Q-point) fixes I_B, I_C and V_{CE} values to be supplied to the transistor when no signal is applied.
4. In a small signal amplifier, the signal amplitude makes the Q-point to swing on the linear portion of the characteristics.
5. A large signal amplifiers is the one in which the signal amplitude, swings the Q-point even over the non-linear portion of the characteristics. This produces distortion.
6. In push-pull amplifier, the signal to be amplified is converted to two 180 degree out of phase signals that are applied simultaneously to the inputs of two transistors. The amplified output signal is developed across a transformer connected between the collectors of two transistors.
7. Tuned amplifiers commonly use *LCR*-tuned circuits and have a frequency response similar to that of the parallel tuned *LCR* filter.

4.9 TERMINAL QUESTIONS

1. Why do you select the operating point on the linear portion of the characteristics ?
2. What is meant by biasing ? Which biasing is the most commonly used?
3. If in the SAQ 1, R_2 is increased by 50% then

   (a) V_{R2} will.....b) V_{RE} will.....

   (c) I_C will..... d) V_C will.....
4. Fill in the gap by choosing the correct option.

   (a) If in an *RC* coupled amplifier the value of a coupling capacitor is increased to twice the original value, the low frequency response of the amplifiers would be..... (worse/remains same/better).

   (b) In the above case the high frequency response would be.....(worse/remains same/better).

   (c) If a capacitor is connected across the output terminals of an *RC*-coupled amplifier, its low frequency response would be.....(worse/remains same/better) and high frequency response would be.....(worse/remains same/better).
5. In class B push pull amplifier battery supply is 5 volts, output power is 400 mW and maximum collector dissipation of each transistor is 100 mW. Calculate peak collector current.

4.10 SOLUTIONS/ANSWERS

SAQs

1. a) decrease b) decrease

   c) decrease d) increase

2. The overall voltage gain in dB of three-stage amplifier is given as

$$A_{dB} = A_{dB1} + A_{dB2} + A_{dB3}$$

We are given the voltage gains of the individual stages as ratios. So, we should first find the gains of the individual stages in decibels. Thus

$$A_{dB1} = 20 \log_{10} 30 = 29.54 \text{ dB}$$

$$A_{dB2} = 20 \log_{10} 50 = 33.98 \text{ dB}$$

$$A_{dB3} = 20 \log_{10} 80 = 38.06 \text{ dB}$$

Therefore,

$$A_{dB} = 29.54 + 33.98 + 38.06 = 101.58 \text{ dB}$$

Using Eq. (4.23), the overall voltage gain is

$$A = A_1 \times A_2 \times A_3$$

$$= 30 \times 50 \times 80 = 120\,000$$

Therefore, the overall voltage gain in dB is

$$A_{dB} = 20 \log_{10} 120\,000 = 101.58 \text{ dB}$$

3. f_r is given by Eq. (4.36).

Here, $L = 10^{-4}$H, $C = 10^{-10}$F

$$f_r = \frac{1}{2\pi\sqrt{10^{-4} \times 10^{-10}}}$$

Bandwidth is obtained from Eq.(4.35).

$$BW = \frac{f_r}{Q}$$

where Q is Q-factor of LC circuit.

You know from Unit 2 of Block 1 that Q is given by the following relation

$$Q = \frac{R}{\omega_{rL}} \quad or \quad Q = R\,\omega_{rC}$$

The equivalent resistance across the LC circuit is the transistor output resistance in parallel with the load resistance, that is

$$R = \frac{1}{100\text{ k}\Omega} + \frac{1}{100\text{ k}\Omega} = 1 = 50\text{ k}\Omega..$$

or $Q = R\,\omega_{rC} \qquad (\because \omega_o = 2\pi f_0 = 100)$

$$= 50 \times 10^3 \times 10^7 \times 10^{-10} = 50$$

So,

$$BW = \frac{1.6}{50}\text{ MHz} = 32\text{ kHz}.$$

- state the conditions under which a feedback amplifier works as an oscillator,
- state the classification of oscillators,
- explain the working of *LC* and *RC* oscillators.

5.2 CONCEPT OF FEEDBACK

Feedback simply means transferring a portion of the energy from the output of a device back to its input. In other words, feedback is the process of taking a part of output signal and feeding it back to the input circuit. Look at the block diagram shown in Fig.5.1. Let A be the gain of the amplifier when there is no feedback.

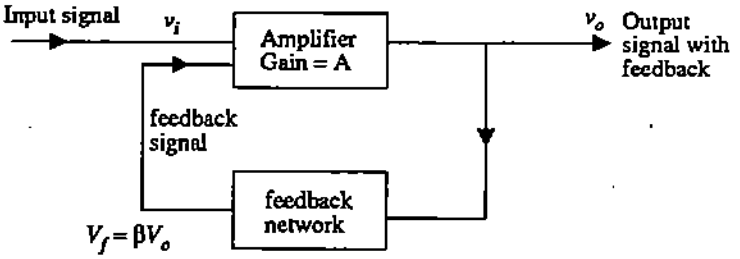


Fig.5.1: Schematic diagram of feedback amplifier.

A portion βV_o where $\beta \leq 1$, is then applied back to the amplifier input. The actual input to the amplifier thus consists of the sum of the signal voltage V_i plus the feedback voltage $V_f = \beta V_o$. We call β as the feedback fraction ($= V_f/V_o$).

So the total input voltage with feedback = $= V_i + \beta V_o$

The output voltage with this input is $V_o = (V_i + \beta V_o) A$

i.e. $V_o = AV_i + A \beta V_o$

as $V_o - A \beta V_o = AV_i$

$$V_o (1 - A\beta) = AV_i$$

$$\therefore \quad \text{Gain with feedback, } A_f = \frac{V_o}{V_i} = \frac{A}{1 - A\beta} \qquad (5.1)$$

5.3 NEGATIVE FEEDBACK AND ITS EFFECT ON AMPLIFIER PERFORMANCE

In Eq. (5.1) if β is negative, then the feedback signal is out of phase with the applied signal. In such a case, the net input voltage to the amplifiers becomes the difference of the external input voltage and the feedback voltage. Since the net input to the amplifier is reduced the output of the amplifier also decreases. In other words, the gain of the amplifier reduces because of the feedback. Such a feedback is called **negative or degenerative feedback**. By putting β as a negative quantity into Eq.(5.1) you will get the gain with negative feedback as

$$A_f = \frac{A}{1 - A(-\beta)} = \frac{A}{1 + A\beta} \qquad (5.2)$$

Since you are dividing A by a positive quantity obviously $A_f < A$. Thus negative feedback reduces the gain of the amplifier.

Before moving further solve the following SAQ to see for yourself how the gain is reduced.

SAQ 1

Calculate the gain of a negative-feedback amplifier with an internal gain, $A = 100$, and feedback factor $\beta = 1/10$.

In the last unit we have discussed the frequency response of an amplifier. The difference $(f_2 - f_1)$ is called the bandwidth (BW) of the amplifier. For an amplifier the product of gain and BW, called gain bandwidth product remains the same i.e. $A \times BW$ = constant. Since the gain of the amplifier is decreased with negative feedback, to get the product $A_f \times BW$ same as before, BW has to increase. In other words, the bandwidth of the amplifier increases with negative feedback. Fig.5.2 shows the frequency response of the amplifier both with and without feedback.

In Eq. (5.2) you can see that if $A\beta$ is very large compared to unity in the denominator, then 1 can be neglected in comparision with AB. So Eq. (5.2) reduces to

$$A_f = \frac{A}{A\beta} = \frac{1}{\beta} \tag{5.3}$$

Since β does not depend upon the parameters of the active device that you have used in the amplifier, such as a transistor, the gain with feedback, A_f is almost independent of the actual gain A. On the other hand, A is dependent upon the transistor parameters. Thus by introducing negative feedback one can have the gain to be completely independent of transistor parameters. This is known as stabilization of amplifier gain.

Likewise other effects of negative feedback are, reduction in distortion, reduction in noise, modification of the input and output resistances of the amplifier etc.

Thus, we have seen that the gain of an amplifier is reduced when negative feedback is used. However, the negative feedback improves the performance of the amplifier from so many other points of view. The advantages of negative feedback are listed as follows :

(i) It increases the bandwidth

(ii) It improves the stability of amplifier gain

(iii) It reduces distortion

(iv) It increases the input impedence

(v) It decreases the output impedence.

5.4 POSITIVE FEEDBACK AND OSCILLATIONS

When the feedback voltage is in phase with the input signal, then it adds to the input signal. In this case β is positive and the feedback is termed as **positive or regenerative feedback**. You can observe that when β is positive, the gain with feedback is given by

$$A_f = \frac{A}{1 - A\beta} \tag{5.4}$$

Since A is divided by a number less than unity $A_f > A$. So positive feedback increases the gain of an amplifier. This in turn reduces the bandwidth because you know that the product (Gain × BW) is constant.

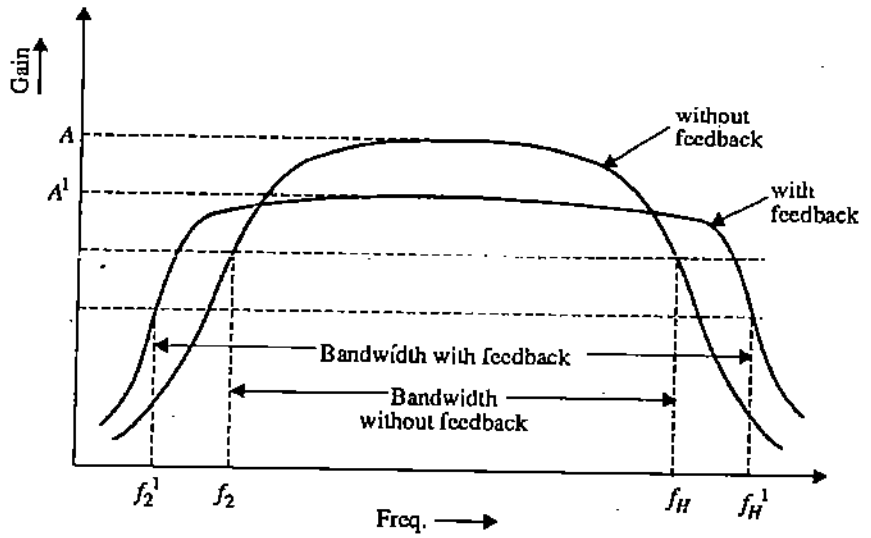


Fig.5.2: Frequency response of feedback amplifier.

is lost during each swing. The amplitude of each half-cycle goes on decreasing. Ultimately, the pendulum comes to rest, though it may like a long time. The oscillations of the pendulum are said to be damped.

A practical *LC* circuit deviates from the ideal one. The inductor coil will have some resistance, and the dielectric material of the capacitor will have some resistance, and the dielectric material of the capacitor will have some leakage. Because of these factors, some energy loss takes place during each cycle of the oscillation. As a result of this loss, the amplitude of oscillation decreases continuously and ultimately the oscillations die down. Thus, we find that a tank circuit by itself is capable of producing oscillations, but they are damped as shown in Fig.5.5e.

Frequency of Oscillations in an *LC* Circuit

In *LC* circuit, the constants of the system are the inductance and capacitance values. The frequency of oscillation is the same as the resonant frequency of the tank circuit. It is given by

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{5.4}$$

Sustained Oscillations

The oscillations of a pendulum can be maintained at a constant level, if we supply additional energy to it from time to time, to overcome the effect of the losses.

The oscillations of an *LC* circuit can also be maintained at a constant level in a similar way For this, we have to supply a spurt of pulse of energy at the right time in each cycle. The resulting "undamped oscillations" are called sustained oscillations, as shown in Fig.5.6. Such sustained oscillations (or continuous waves) are generated by the electronic oscillator circuits.

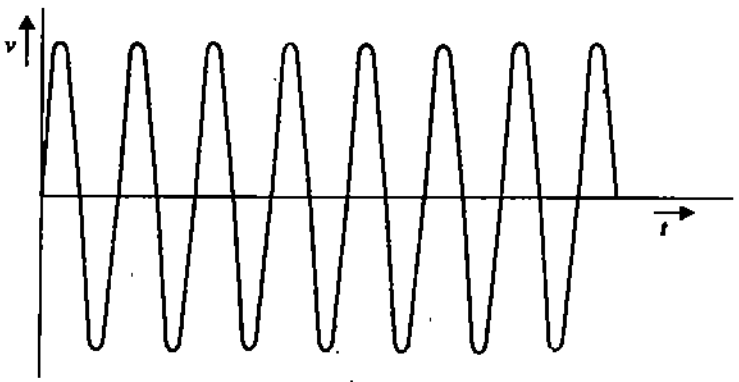


Fig.5.6: Sustained oscillations.

There are many varieties of *LC*-oscillator circuits. All of them have following three features in common :

(i) They must contain an active device (transistor or tube) that works as an amplifier.

(ii) There must be positive feedback in the amplifier.

(iii) The amount of feedback must be sufficient to overcome the losses.

5.4.3 Positive Feedback Amplifier as an Oscillator

The main application of positive feedback is in oscillators. An oscillator generates ac output signal without any input ac signal. A part of the output is fed back to the input; and this feedback signal is the only input to the internal amplifier.

To understand how an oscillator produces an output signal without an external input signal, let us consider Fig.5.7a. The voltage source v drives the input terminals YZ of the internal amplifier (with voltage gain A). The amplified signal AV drives the feedback network to produce feedback voltage $A\beta$. This voltage returns to the point X. If the phase shift due to the amplifier and feedback network is correct, the signal at point X will be exactly in phase with the signal driving the input terminals YZ of the terminal amplifier.

The action of an oscillator is explained a little later. For the time being, assume that we connect points X and Y, and remove voltage source v. The feedback signal now drives the input terminals YZ of the amplifier (see Fig.5.7b). If $A\beta$ is less than unity, $A\beta v$ is less than v, and the output signal will die out as shown in Fig.5.7c. This happens because enough voltage is not returned to the input of the amplifier. On the other hand, if $A\beta$ is greater than unity, $A\beta v$ is greater than v, and the output voltage builds up as shown in Fig.5.7d. Such oscillations are called growing oscillations. Finally, if $A\beta$ equals unity, no change occurs in the output: we get an output whose amplitude remains constant, as shown in Fig.5.7e.

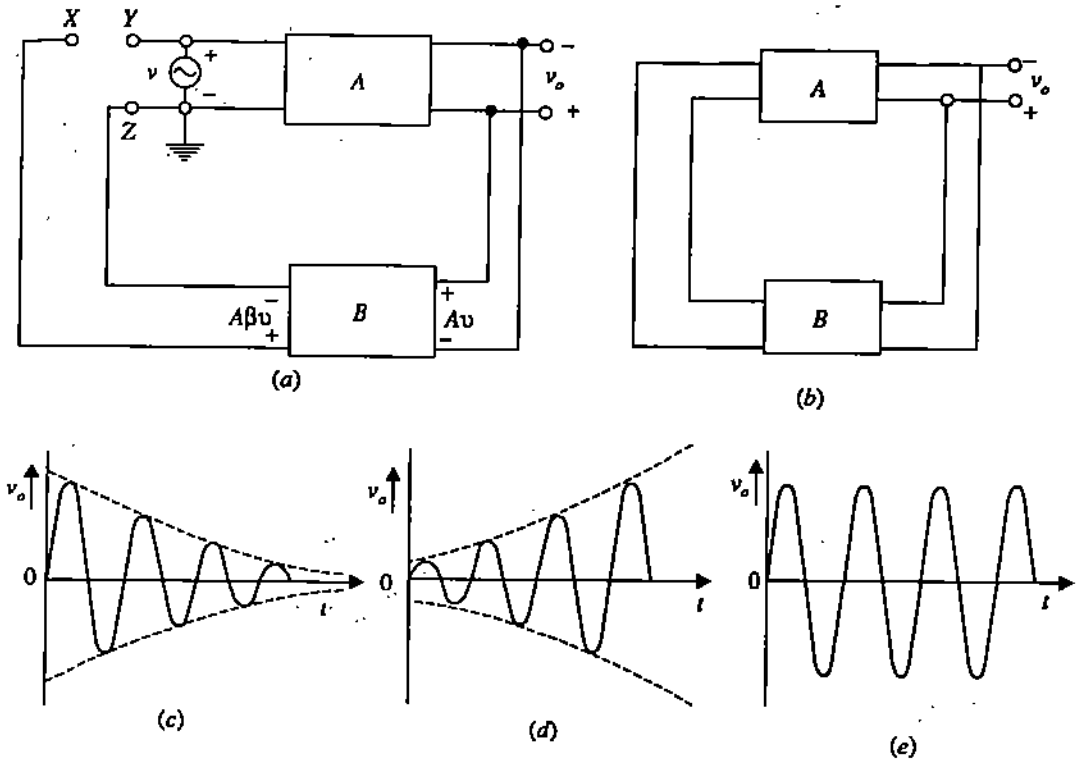


Fig.5.7: Proper positive feedback in an amplifier makes it an oscillator.

To find the necessary condition for the sustained oscillations, refer to Eq. (5.4) for the overall gain of the amplifier when the feedback is positive,

$$A_f = \frac{A}{1 - A\beta} \tag{5.5}$$

It can now be seen that if $A\beta = 1$ $A_f = \infty$. The gain becoming infinity means that there is output without any input. In other words, the amplifier becomes an oscillator. The condition,

$$A\beta = 1, \tag{5.6}$$

known as Barkhausen criterion of oscillation, is the necessary condition.

5.5 *LC* OSCILLATORS

LC oscillators or resonant-circuit oscillators are widely used for generating high frequencies. With practical values of inductors and capacitors, it is possible to produce frequencies as high as 500 MHz. The oscillators used in rf generators, radio and TV receivers, high-frequency heating, etc. are *LC* oscillators. Such an oscillator has an amplifier, an *LC* resonant circuit and a feedback arrangement. There is a large variety of *LC*-oscillator circuits. Here, we shall discuss only a few important ones.

5.5.1 Tuned-collector Oscillator

Fig.5.8 shows a basic *LC*-oscillator circuit. It is called tuned-collector oscillator, because the tuned circuit is connected to the collector. We have used a transformer here. The

Multiplying by $\frac{h_{oe}}{j\omega C_1}$ on both sides, we have

$$\frac{h_{fe}}{h_{ie}} \times \frac{M}{C_1} - \frac{1}{j\omega C_1} - R - j\omega L_1 = \frac{(R + j\omega L_1) h_{oe}}{j\omega C_1}$$

or

$$\frac{h_{fe}}{h_{ie}} \times \frac{M}{C_1} = R + j\left(\omega L_1 - \frac{1}{\omega C_1}\right) + \left[\frac{-jh_{oe} R}{\omega C_1} + \frac{L_1 h_{oe}}{C_1}\right] \quad (5.15)$$

Equating the real parts in Eq. (5.15), we get

$$\frac{h_{fe}}{h_{ie}} - \frac{M}{C_1} = R + -\frac{L_1 h_{oe}}{C_1}$$

or $$\boxed{\frac{h_{fe}}{h_{ie}} = \frac{R C_1 + h_{oe} L_1}{M}} \quad (5.16)$$

Eq. (5.16) gives the condition for sustained oscillation. Equating the imaginary part in Eq. (5.15),

we get

$$\omega L_1 - \frac{1}{\omega C_1} - \frac{h_{oe} R}{\omega C_1} = 0$$

or $$\omega^2 = \frac{1}{L_1 C_1}\left[1 + h_{oe} R\right]$$

or $$\boxed{\omega^2 = \omega_0^2 (1 + h_{oe} R)} \quad (5.17)$$

$$\left[\text{where } \omega_o^2 = \frac{1}{L_1 C_1}\right]$$

Eq. (5.17) gives the frequency of oscillation. Thus equation shows that the frequency of oscillation exceeds the frequency of resonance of the tuned circuit.

5.5.2 Hartley Oscillator

The Hartley oscillator is one of the simplest types of oscillator circuits. In this circuit only one coil is used, which is tapped such that a portion L_1 of the coil is in the collector circuit, while L_2 is in the base circuit. The amplified energy in the collector section is fed back to

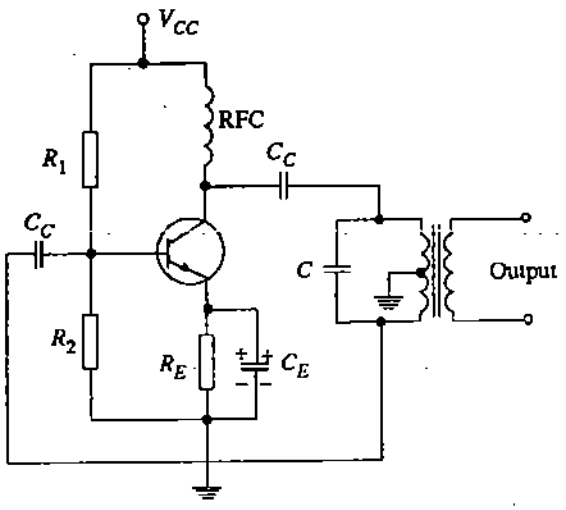


Fig: 5.10: Hartley Oscillator.

the base by means of inductive coupling and amount of coupling will depend upon the number of turns in L_1 and L_2. Fig.5.10 shows a Hartley oscillator circuit.

An *RFC* (radio frequency choke) permits an easy flow of dc current. At the same time, it offers very high impedence to high frequency currents. In other words, an *RFC* ideally looks like a dc short and an ac open. The presence of the coupling capacitor C_c in the output circuit of the Hartley oscillator does not permit the dc currents to go to the tank circuit. The radio-frequency energy developed across the *RFC* is capacitively coupled to the tank circuit through the capacitor C_c.

The frequency of oscillation can be calculated in a manner similar to the one described in case of tuned collector oscillator. It is given by

$$\omega = \omega_0 \sqrt{1 - \frac{X_1 X_2}{1 - h_{ie} h_{oe}}}$$

Where $\omega L_1 = X_1$ and $\omega L_2 = X_2$.

5.5.3 Colpitts Oscillator

The Colpitts oscillator in Fig.5.11 is a superb circuit. It is widely used in commercial signal generators above 1 MHz. The oscillator is similar to the Hartley oscillator given in Fig.5.10. The only difference is that the Colpitts oscillator uses a split-tank capacitor instead of a split-tank inductor. The *RFC* has the same function as in the Hartley oscillator. The voltage developed across the capacitor C_2 provides the regenerative feedback required for the sustained oscillations. The values of L, C_1 and C_2 determine the frequency of oscillation. The frequency of oscillation is given by

$$f = \frac{1}{2\pi \sqrt{LC}} \tag{5.18}$$

where,

$$C = \frac{C_1 C_2}{C_1 + C_2} \tag{5.19}$$

since C_1 and C_2 are in series.

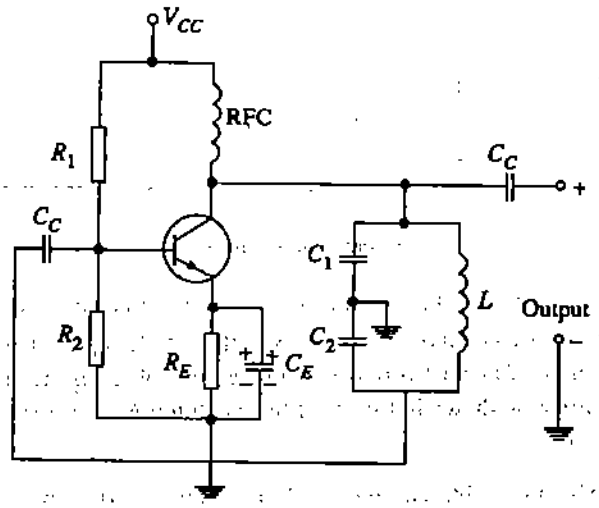


Fig.5.11: Colpitts oscillator using a transistor.

5.6 *RC* OSCILLATORS

Till now we have discussed only those oscillators which use an *LC*-tuned circuit. These tuned circuit oscillators are good for generating high frequencies. But for low frequencies (say, audio frequencies), the *LC* circuit becomes impracticable. *RC* oscillators are more suitable. There are many types of *RC* oscillators, but following two are most important:

(i) Phase-shift oscillator

(ii) Wein bridge oscillator

Basic Principles of *RC* Oscillators

We know that a single stage of an amplifier not only amplifies the input signal but also shifts its phase by 180°. If we take a part of the output and feed it back to the input, a negative feedback takes place. The net output voltage then decreases. But for producing oscillations we must have positive feedback (of sufficient amount). Positive feedback occurs only when the feedback voltage is in phase with the original input signal. This condition can be achieved in two ways. We can take a part of the output of a single stage amplifier (giving a phase shift of 180°) and then pass it through a phase-shift network giving an additional phase shift of 180°. Thus a total phase shift of 180° +180° = 360° (which is equivalent to a phase shift of 0°) occurs, as the signal passes through the amplifier and the phase-shift network. This is the principal of a phase-shift oscillator.

Another way of getting a phase shift of 360° is to use two stages of amplifiers each giving a phase shift of 180°. A part of this output is fed back to the input through a feedback network without producing any further phase shift. This is the principle of a wein bridge oscillator.

5.6.1 Phase-Shift Oscillator

Fig.5.12 shows a phase-shift oscillator.

As shown in the figure, the phase of the signal at the input gets reversed when it is amplified by the amplifier. The output of the amplifier goes to a feedback network. The

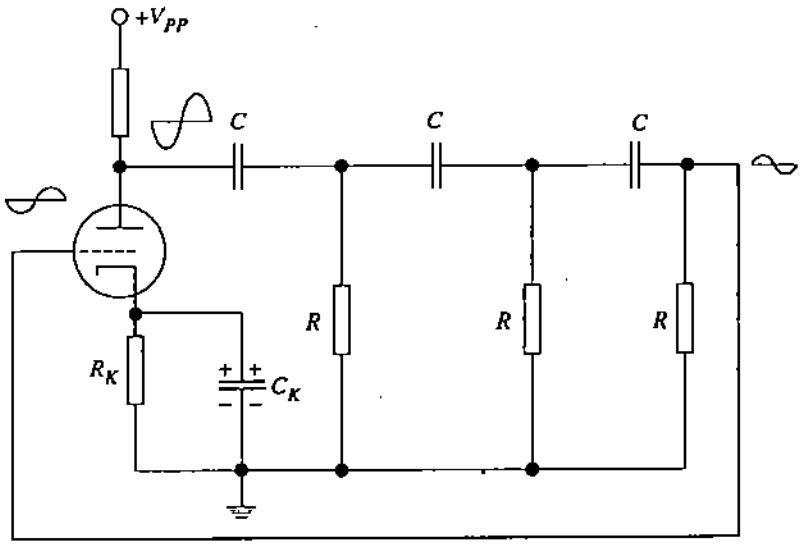


Fig.5.12 : Phase-shift oscillator.

feedback network consists of three identical *RC* sections. Each *RC* section provides a phase shift of 60°. Thus a total of 60° × 3 = 180° phase shift is provided by the feedback network. The output of this network is now in the same phase as the originally assumed input to the amplifier, as shown in figure. If the condition $A\beta = 1$ is satisfied, oscillations will be maintained.

It may be shown by a straightforward (but a little complicated) analysis that the frequency at which the *RC* network provides exactly 180° phase-shift is given by

$$f = \frac{1}{2\pi R C\sqrt{6}} \qquad (5.20)$$

This must then be the frequency of oscillation.

SAQ 3

A transistor phase-shift oscillator uses three identical *RC* sections in the feedback network. The values of the components are R =100 k and C=0.01μ F. Calculate the frequency of oscillation.

5.6.2 Wein Bridge Oscillator

The Wein bridge oscillator is a standard circuit for generating low frequencies in the range of 10 Hz to about 1 MHz. It is used in all commercial audio generators. Basically, this oscillator consists of two stages of *RC*-coupled amplifier and a feedback network. The block diagram of Fig.5.13 explains the principles of working of this oscillator.

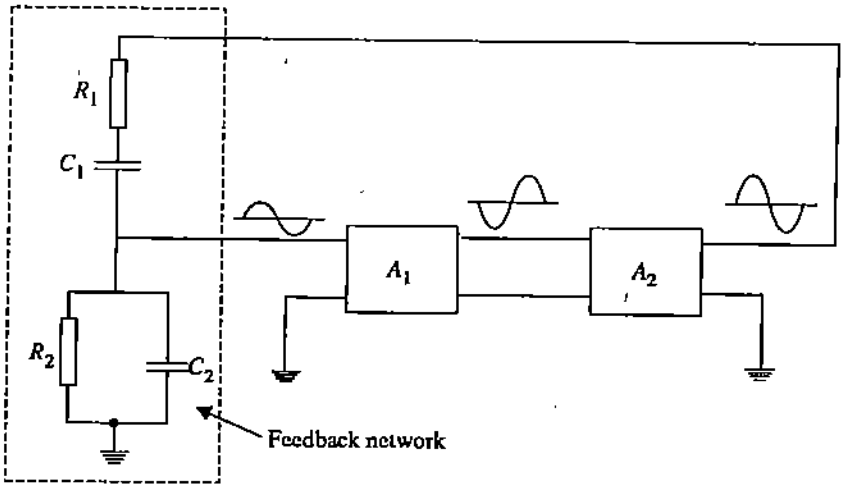


Fig.5.13: Block diagram of a basic Wein bridge oscillator.

Here, the blocks A_1 and A_2 represent two amplifier stages. The output of the second stage goes to the feedback network. The voltage across the parallel combination $C_2 R_2$ is fed to the input of the first stage. The net phase shift through the two amplifiers is zero. Therefore, it is evident that for the oscillation to be maintained, the phase shift through the coupling network must be zero. It can be shown that this condition occurs at a frequency given by

$$f_o = \frac{1}{2\pi \sqrt{R_1 C_1 R_2 C_2}} \tag{5.21}$$

To have a gain we add some amount of negative feedback. The addition of negative feedback modifies the circuit in Fig.5.13 to that shown in Fig.5.14. The same circuit is redrawn as in Fig.5.15.

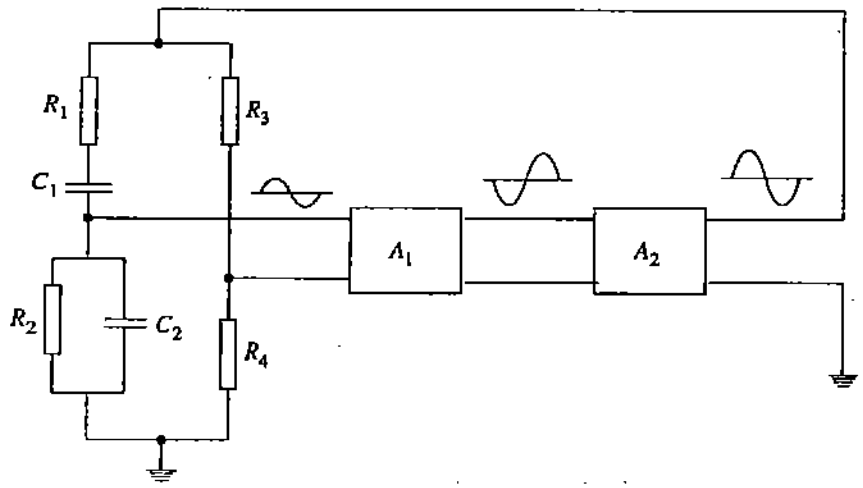


Fig.5.14: Circuit in Fig. 5.13 modified to include negative feedback.

You may now see why this circuit is called a bridge oscillator. In this circuit, the resistors R_3 and R_4 provide the desired negative feedback. The two blocks in Fig.5.14 representing the two stages of the amplifier are replaced by a single block in Fig.5.15.

We can have a continuous variation of frequency in the oscillator by varying the two capacitors C_1 and C_2 simultaneously. These capacitors are variable air-gang capacitors. We can change the frequency range of the oscillator by switching into the circuit different values of resistors R_1 and R_2.

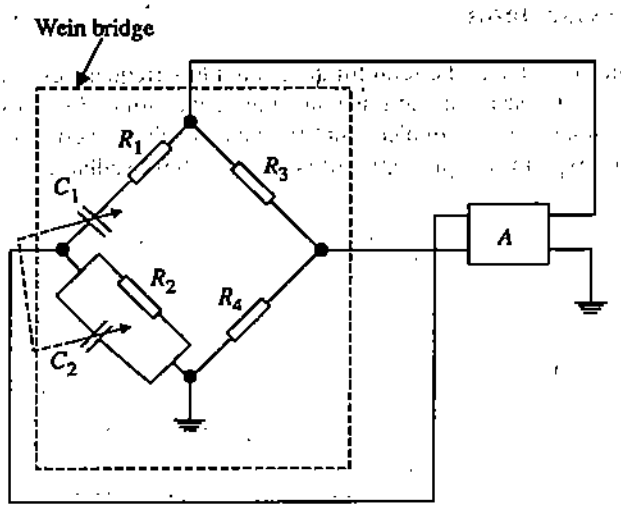


Fig.5.15: Circuit in Fig. 5.14 is redrawn to show the presence of a "bridge" in Wein bridge oscillator.

SAQ 4

The RC network of a Wein bridge oscillator consists of resistors and capacitors of values $R_1 = R_2 = 220$ K and $C_1 = C_2 = 250$ pF. Calculate the frequency of Oscillations.

5.7 SUMMARY

(1) An amplifier in which a portion of the output voltage or current is fed back to the input is called a feedback amplifier.

(2) If the feedback signal is in phase with the applied signal and aids it, positive or regenerative feedback takes place.

(3) If the feedback signal is opposed to the applied signal (i.e. out of phase), negative or degenerative feedback takes places.

(4) Gain increases with positive feedback, which may lead to oscillations.

(5) Negative feedback decreases the gain, and also distortion.

(6) An oscillator acts as energy converter which changes direct current energy into alternating current energy.

(7) Essential parts of an oscillator are (i) the frequency determining network (ii) source of dc energy and (iii) a feedback circuit to provide positive feedback.

(8) Hartley oscillator uses a tapped coil in the feedback circuit.

(9) Colpitt's oscillator uses a tapped capacitance network in the feedback circuit. It has better frequency stability than Hartley oscillator.

(10) A Wein bridge oscillator is an RC oscillator whose frequency of oscillation can be varied over a wide range.

5.8 TERMINAL QUESTIONS

(1) Gain of an amplifier without feedback is 10^3. If the gain with negative feedback is 10^2, what is the feedback ratio ?

(2) An amplifier with negative feedback has a voltage gain of 100. It is found that without feedback, an input signal of 50 mV is required to produce a given output; whereas with feedback, the input signal must be 0.6 V for the same output. Calculate the value of A and β.

(3) What is meant by stabilization of gain ? How is it achieved with negative feedback ?

(4) What is meant by loop gain ?

(5) A Wien bridge oscillators uses 10 k resistors and 4.70 nF capacitors in its bridge circuit. What is the frequency of oscillation ?

5.9 SOLUTIONS/ANSWERS

SAQ's

1. The gain of the feedback amplifier is given by

$$A_f = \frac{A}{1 + A\beta}$$

Here, A = 100; β = 1/10 =0.1. Hence

$$A_f = \frac{100}{1 + 100 \times 0.1} = \frac{100}{1 + 10} = \frac{100}{11}$$

$$= 9.09$$

2. (i) Decreases, Increases

(ii) $\frac{1}{\beta} = \frac{1}{0.01} = 100$

(iii) Reduces

(iv) Degenerative feedback.

3. The frequency of oscillation of a phase-shift oscillator is given as

$$f_o = \frac{1}{2\pi R C \sqrt{6}}$$

Here, R =100 k =10^5 ; C = 0.01 μ F = 10^{-8}F.

Therefore,

$$f_o = \frac{1}{2 \times 3.141 \times 10^5 \times 10^{-8} \times 2.45} = 64.97 \text{ Hz}$$

4. For a Wein bridge oscillator, the frequency of oscillation is given as

$$f_o = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}} = \frac{1}{2\pi RC}$$

where $R_1 = R_2 = R$, and $C_1 = C_2 = C$.

Here, R = 220 K = 2.2×10^5 ; C = 250 pF = 2.5×10^{-10} F .

Therefore,

$$f_o = \frac{1}{2 \times 3.141 \times 2.2 \times 10^5 \times 2.5 \times 10^{-10}}$$

$$= 2893.7 \text{ Hz}$$

$$= 2.89 \text{ kHz} .$$

TQ's

1. $A' = \frac{A}{1 + A\beta}$ $A' = 100, A = 1000$

$$100 = \frac{1000}{1 + A\beta}$$

The output from a d.c. power unit on its own is usually unsatisfactory for two reasons: firstly because it usually carries a small amount of **a.c. ripple** superimposed on the d.c. voltage, so that if it is used to supply an audio amplifier it would probably give rise to some audible 'hum' from the loudspeaker. Secondly the internal resistance of the d.c. power unit is usually higher than desirable, implying that the voltage output can be significantly affected by variations in the current drawn from the unit. The change in output voltage per unit change of output current is called the **regulation** of the d.c. source. This is just another way of referring to the output resistance of the circuit. The regulating circuitry added to the d.c. power unit in a regulated d.c. supply reduces the ripple and improves the regulation.

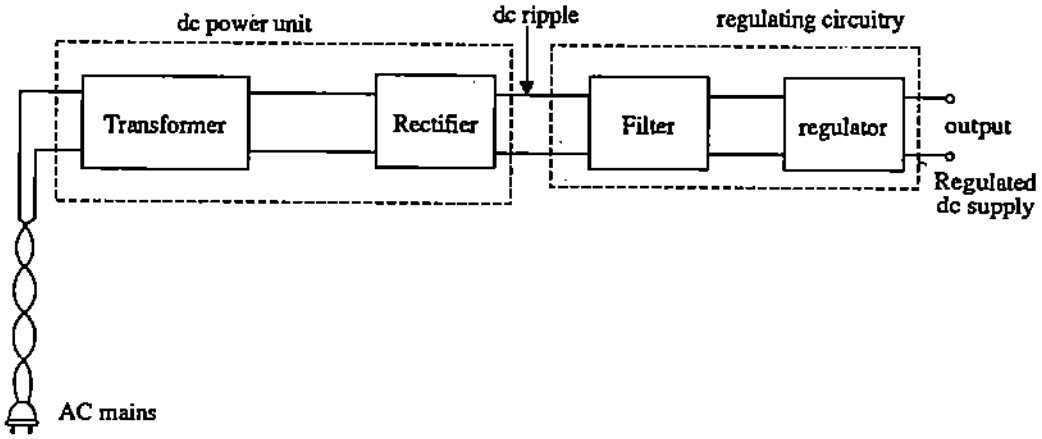


Fig.6.1: The block diagram of power supply. It consists of a d.c. power unit, which converts the a.c. supply to a d.c. voltage plus some mains ripple ; followed by circuitry which reduces the ripple and regulates the output voltage.

In this unit we examine the electrical principles involved in transforming ac power to dc power and discuss several techniques of transformation. But before doing this we study the sources of electrical power viz. voltage and current sources.

In the next unit you will come across many testing, measuring and indicating instruments. There we will only present and explain the relevant basic details of these instruments. This would help the student to familiarize himself with these instruments so that he can use them effectively.

Objectives

After going through this unit you will be able to:

- explain and use correctly the following terms : voltage source, current source, half-wave rectification, full-wave rectification, bridge rectifier, ripple, load regulation, line regulation,
- draw the circuit diagram and explain the working of half-wave rectifier, centre-tapped full wave rectifier and bridge rectifier,
- derive in case of half-wave and full-wave rectifiers, the expressions for output dc voltage, average or dc current, rms current, ripple factor and rectifier efficiency,
- explain the need of filters in dc power supply,
- explain with the help of suitable waveforms the working of rectifiers using shunt-capacitor, series inductor and *LC* filters,
- explain the function of each part of a power supply.

6.2 POWER SOURCE

The basic purpose of a source is to supply power to a load. The source may supply either dc or ac. Some dc sources are battery and rectification type dc supply. Similarly, example of ac source is an oscillator. Source of power can also be classified into two; like voltage source and current source about which we will study in this section.

All power sources have some internal impedance (or resistance). It is due to this internal impedance that the source does not behave ideally. When a voltage source supplies power to a load, its terminal voltage (voltage available at its terminals) drops. A cell used in a torch has a voltage of 1.5 V across its two terminals when nothing is connected to it. However, when connected to a bulb, its voltage becomes less than 1.5 V. Such a reduction in the terminal voltage of the cell may be explained as follows.

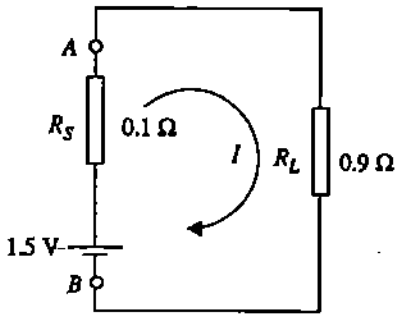


Fig. 6.2 : A cell connected to a bulb.

Fig.6.2 shows a cell of 1.5 V connected to a bulb. When we say "cell of 1.5 V", we mean a cell whose open-circuit voltage is 1.5 V. Here the bulb is replaced by a load resistor R_L (of, say, 0.9 Ω), and the cell is replaced by a constant voltage source of 1.5 V in series with the internal resistance R_s (of, say, 0.1 Ω). The total resistance in the circuit is now 0.1 Ω + 0.9 Ω = 1.0 Ω. Since the net voltage that sends current into the circuit is 1.5 V, the current in the circuit is

$$I = \frac{V}{R} = \frac{1.5\text{V}}{1.0\,\Omega} = 1.5\text{ A}$$

The terminal voltage (the voltage across the terminals AB) of the cell is same as the voltage across the load resistor R_L. Therefore,

$$V_{AB} = I \times R_L = 1.5\text{A} \times 0.9\,\Omega = 1.35\text{V}$$

The voltage that drops because of the internal resistance is

$$1.5 - 1.35 = 0.15\text{ V}$$

Note that, if the internal resistance of the cell were smaller (compared to the load resistance), the voltage drop would also have been smaller than 0.15 V.

6.2.1 Voltage Source

Consider an ac source. Let V_S be its open-circuit voltage (i.e.the voltage which exists across its terminals when nothing is connected to it), and Z_S be its internal impedance. Let it be connected to a load impedance Z_L whose value can be varied, as shown in Fig.6.3.

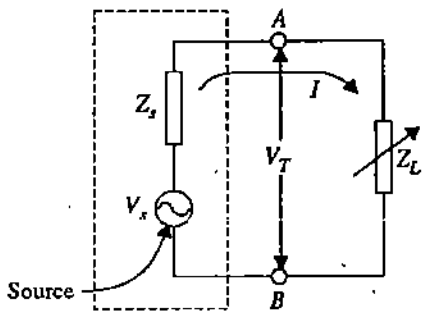


Fig.6.3: A variable load connected to an ac source.

Now, suppose Z_L is infinite. It means that the terminals AB of the source are open-circuited. Under this condition, no current can flow. The terminal voltage V_T is obviously the same as the emf V_S, since there is no voltage drop across Z_S. Let us now

connect a finite load impedance Z_L, and then go on reducing its value. As we do this, the current in the circuit goes on increasing. The voltage drop across Z_S also goes on increasing. As a result, the terminal voltage V_T goes on decreasing.

For a given value of Z_L, the current in the circuit is given as

$$I = \frac{V_S}{Z_S + Z_L}.$$

Therefore, the terminal voltage of the source , which is the same as the voltage across the load, is

$$V_T = I \times Z_L = \frac{V_S}{Z_S + Z_L} \times Z_L = \frac{V_S}{1 + Z_S/Z_L} \tag{6.1}$$

From the above equation, we find that if the ratio Z_S/Z_L is small compared to unity, the terminal voltage V_T remains almost the same as the voltage V_S. Under this condition, the source behaves as a good voltage source. Even if the load impedance changes, the terminal voltage of the source remains practically constant (provided the ratio Z_S/Z_L) is quite small). Such a source is said to be a "good (but not ideal) voltage source".

Ideal Voltage Source

It would have been ideal, if the terminal voltage of a source remains fixed whatever be the load connected to it. In other words, a voltage source should ideally provide a fixed terminal voltage even though the current drawn (or load resistance) may vary. In Eq.6.1, to make the terminal voltage V_T fixed for any value of Z_S, the only way is to make the internal impedance Z_S zero. Thus, we infer that an ideal voltage source must have zero internal impedance. The symbolic representation of dc and ac ideal voltage sources are shown in Fig.6.4a and b. The characteristics of an ideal voltage sources is shown in Fig.6.4c. The terminal voltage V_T is seen to be constant at Z_S for all values of load current.

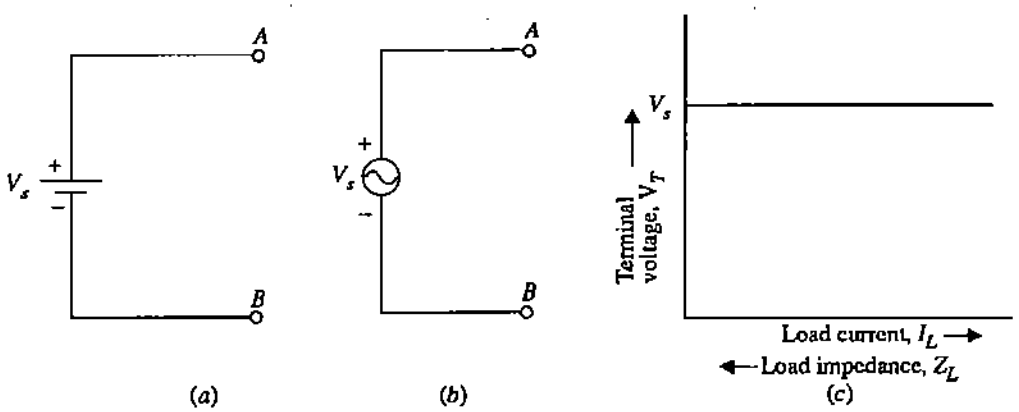


Fig.6.4: Symbolic representation of an ideal voltage source: (a) DC voltage source. (b) AC voltage source. (c) V-I characteristics of an ideal voltage source.

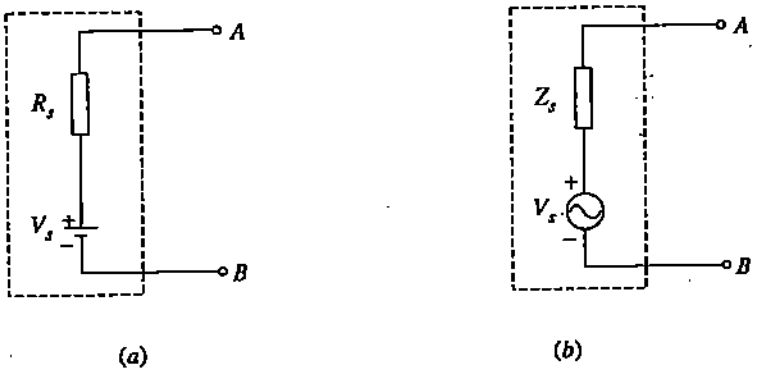
Practical Voltage Source

An ideal voltage source is not practically possible. There is no source which can maintain its terminal voltage constant when its terminals are short-circuited. If it could do so, it would mean that it can supply an infinite amount of power to a short-circuit. This is not possible. Hence, an ideal voltage source does not exist in practice. However, the concept of an ideal voltage source is very helpful in understanding the circuits containing a practical voltage source.

A practical voltage source can be considered to consist of an ideal voltage source in series with an impedance. This impedance is called the internal impedance. The symbolic representation of practical voltage sources are shown in Fig.6.5.

Terminal A and B are the terminals available for making external connections.

No practical voltage source can be an ideal voltage source. Thus, no practical voltage source can have the V-I characteristic as shown in Fig.6.4c. When the load current increases, the terminal voltage of a practical voltage source decreases as shown in Fig.6.6.



(a) (b)

Fig.6.5: Practical voltage source: (a) DC voltage source (b) AC voltage source.

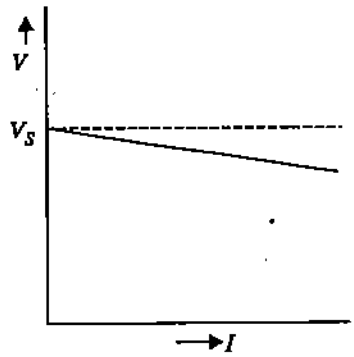
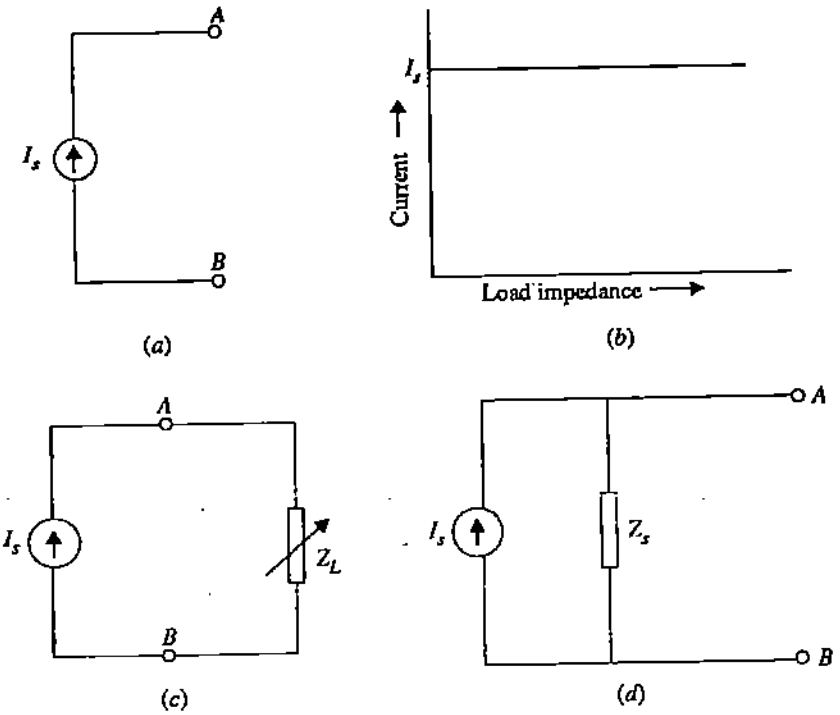


Fig.6.6: V-I characteristics of a practical voltage source.

6.2.2 Current Source

Like a constant voltage source, there may be a constant current source–a source that supplies a constant current to a load even if its impedance varies. Ideally, the current supplied by it should remain constant, no matter what the load impedance is. A symbolic representation of such an ideal current source is shown in Fig.6.7a. The arrow inside the circle indicates the direction in which current will flow in the circuit when a load is connected to the source. Fig.6.7b shows the V-I characteristic of an ideal current source.

Let us connect a variable load impedance Z_L to a constant current source, as shown in Fig.6.7c



(a) (b) (c) (d)

Fig.6.7: (a) Symbol for an ideal current source.(b) V-I characteristic of an ideal current source. (c) A variable load connected to an ideal current source. (d) Symbol for a practical current source.

6.3.2 Half-wave Rectification

In practice most d.c. power units use **full-wave rectification**, which is achieved either by the use of the 'full-wave rectifier' circuit with a centre-tapped transformer winding, or else by a 'bridge rectifier' with a single secondary transformer winding. Both these circuits will be explained after having explained the simpler **half-wave rectification** circuit.

Fig.6.9 shows the circuit of a d.c. power unit with half-wave rectifier where the diode forms a series circuit with the secondary of the transformer and the load resistor R_L.

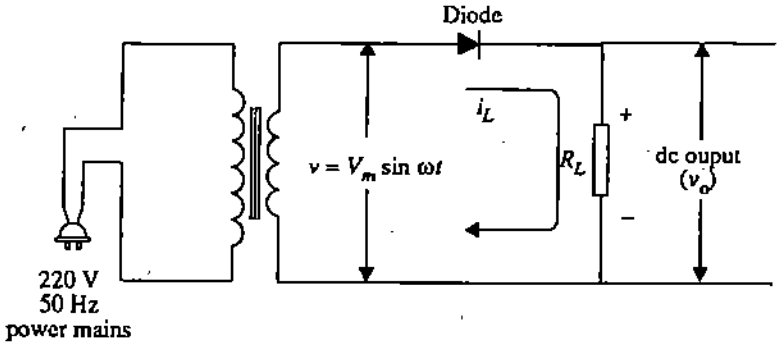


Fig.6.9: A half-wave rectifier circuit consisting of a transformer, a diode and a load resistor.

Let us see how this circuit rectifies ac into dc.

The primary of the transformer is connected to the power mains. An ac voltage is induced across the secondary of the transformer. The voltage may be less than, or equal to, or greater than the primary voltage depending upon the turns ratio of the transformer. We can represent the voltage across the secondary by the equation.

$$v = V_m \sin \omega t \qquad (6.3)$$

Fig.6.10a shows how voltage varies with time. It has alternate positive and negative half-cycles. Voltage V_m is the peak value of this alternating voltage.

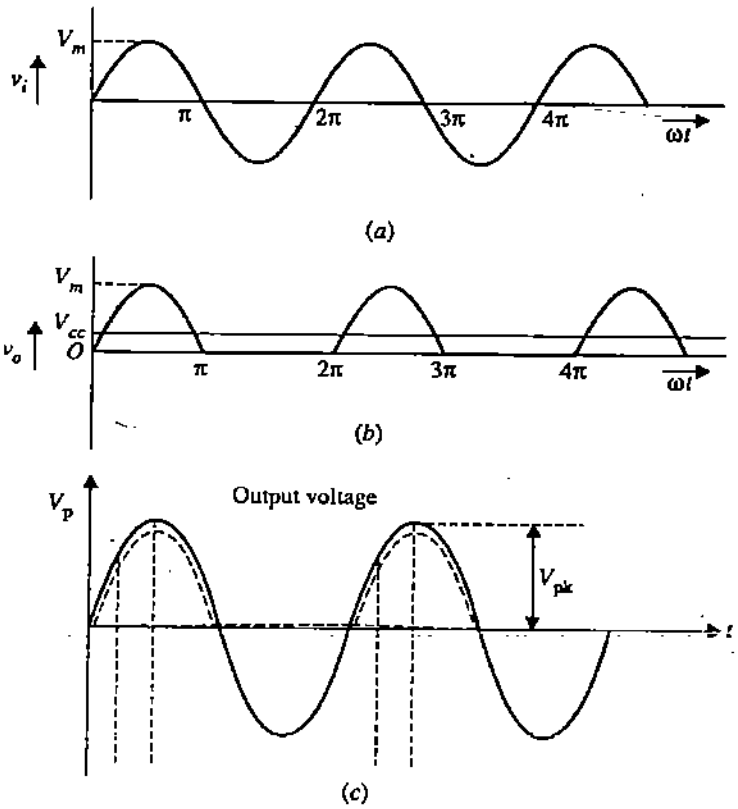


Fig.6.10: Half-wave rectifier: (a) Input voltage waveform (b) Output voltage waveform. (c) The transformer output voltage (input voltage) waveform together with the rectified voltage (output voltage) waveform across the load (shown dashed).

During the positive half-cycle of the input voltage, the polarity of the voltage across the secondary is as shown in Fig.6.11a. This polarity makes the diode forward biased, because it tries to push the current in the direction of the diode arrow. The diode conducts, and a current i_L flows through the load resistor R_L. This current makes the terminal A positive with respect to terminal B. Since a forward-biased diode offers a very low resistance, the voltage drop across it is also very small (about 0.3 V for Ge diode and about 0.7 V for Si diode). Therefore, the voltage appearing across the load terminals AB is practically articularly the same as that the input voltage v_i at every instant. But ideally speaking the situation is slightly different. By solving the following SAQ find out for yourself.

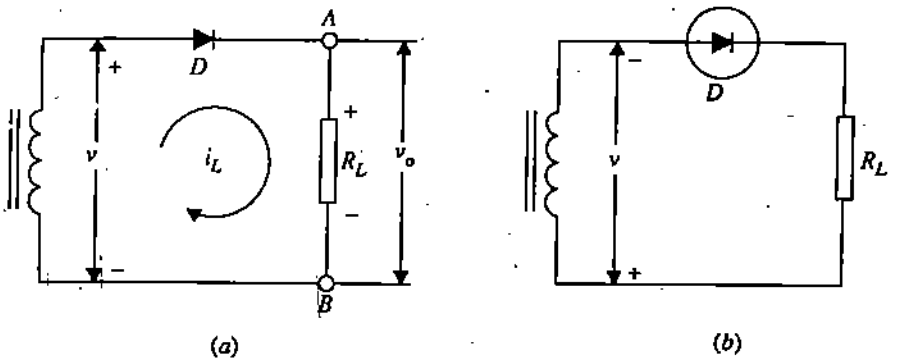


Fig.6.11: Half-wave rectifier circuit : (a) During positive half-cycle; (b) During negative half cycle.

SAQ 2

Fig.6.10(c) shows the transformer output (input voltage) waveform as a continuous line and the voltage across the load resistor (output voltage) as a dashed line. Why the output voltage is less than the input voltage. Give reasons for the difference between the two waveforms.

During the negative half-cycle of the input voltage, the polarity gets reversed. The voltage tries to send current against the direction of diode arrow. See Fig.6.11b. The diode is now reverse biased. It is shown shaded in the figure to indicate that it is non-conducting. Practically no current flows through the circuit. Therefore, almost no voltage is developed across the load resistance. All the input voltage appears across the diode itself. This explains how we obtain the output waveshape as shown in Fig.6.10b

To sum up, when the input voltage is going through its positive half-cycle, the voltage of the output is almost the same as the input voltage. During the negative half-cycle, no voltage is available across the load. The complete waveform of the output voltage v_o across the load is shown in Fig.6.10b. This voltage, though not a perfect dc, is at least unidirectional.

Peak Inverse Voltage

Let us again focus our attention on the diode in Fig.6.11b. During the negative half-cycle of the input, the diode is reverse biased. The whole of the input voltage appears across the diode (as there is no voltage across the load resistance). When the input reaches its peak value V_m in the negative half-cycle, the voltage across the diode is also maximum. This maximum voltage is known as the peak inverse voltage (PIV). It represents the maximum voltage the diode must withstand during the negative half-cycle of the input. Thus for a half-wave rectifier,

$$PIV = V_m \qquad (6.4)$$

Output dc Voltage

The average value of a sine wave (such as that in Fig.6.10a) over one complete cycle is zero. If a dc ammeter (moving coil type) is connected in an ac circuit, it will read zero. (The dc meter reads average value of current in a circuit.) Now, if the dc ammeter is connected in the half-wave rectifier circuit (Fig.6.9), it will show some reading. This indicates that there is some dc current flowing through the load R_L. We can find out the value of this current in a half-wave rectifier circuit.

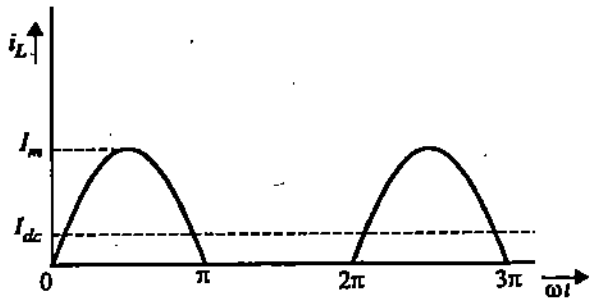


Fig.6.12: Waveform of the current flowing through load R_L in a half-wave rectifier.

In Fig.6.10b, we had plotted the waveform of the voltage across the load resistor R_L. If we divide each ordinate of this curve by the value of resistance R_L, we get the current waveform. This is shown in Fig.6.12. Note that the two waveforms (for current and for voltage) are similar. Mathematically, we can describe the current waveform as follows :

$$i_L = I_m \sin \omega t \text{ ; for } 0 < \omega t < \pi \tag{6.5}$$

$$\text{and } \; i_L = 0 \text{ ; for } \pi < \omega t < 2\pi \tag{6.6}$$

Here, I_m is the peak value of the current i_L. It is obviously related to the peak value of voltage V_m as

$$I_m = \frac{V_m}{R_L} \tag{6.7}$$

since the diode resistance in the conducting state is assumed to be zero. To find the dc or average value of current, we add or integrate the instantaneous values of the current over one complete cycle, i.e. from 0 to 2π (curve repeats itself after the first cycle). Using Eq.6.5 and 6.6 we find the dc current as follows :

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin \omega t \, d(\omega t) + \int_{\pi}^{2\pi} 0 \, d(\omega t)\right]$$

$$= \frac{1}{2\pi}\left[I_m \left\{(-\cos \omega t)\right\}_0^{\pi} + 0\right]$$

$$= \frac{1}{2\pi}\left[I_m \left(-\cos \pi - (-\cos 0)\right)\right]$$

$$= \frac{I_m}{\pi}$$

$$\therefore I_{dc} = \frac{I_m}{\pi} \tag{6.8}$$

The dc voltage developed across the load R_L is

$$V_{dc} = I_{dc} \times R_L = \frac{I_m}{\pi} \times R_L \tag{6.9}$$

While writing Eq. 6.7, we had assumed that

(i) the diode resistance in forward bias is zero, and

(ii) the secondary winding of transformer has zero resistance.

The second assumption is often very near the truth. The winding resistance is almost zero. But, the forward diode-resistance r_d is sometimes not so small. If it is comparable to the load resistance R_L, we must take it into consideration. Eq.6.7 for peak current then gets modified to

$$I_m = \frac{V_m}{(R_L + r_d)} \tag{6.10}$$

The dc voltage across the load resistor R_L, can now be written with the help of Eq.6.7 as

$$V_{dc} = \frac{V_m R_L}{\pi(R_L + r_d)} = \frac{V_m}{\pi\,(1 + r_d/R_L)}$$

$$= \frac{V_m}{\pi}\ (if\ r_d < R_L) \tag{6.11}$$

Example 1

The turns ratio of a transformer used in a half-wave rectifier (such as shown in Fig.6.9) is 12 : 1. The primary is connected to the power mains: 220 V, 50 Hz. Assuming the diode resistance in forward bias to be zero, calculate the dc voltage across the load. What is the PIV of the diode ?

Solution

The maximum (peak value) primary voltage is

$$V_P = \sqrt{2}\ V_{rms} = \sqrt{2} \times 220 = 311\text{V}.$$

Therefore, the maximum secondary voltage is

$$V_m = \frac{1}{12} \times 311 = 25.9\ \text{V}$$

The dc load voltage is

$$V_{dc} = \frac{V_m}{\pi} = \frac{25.9}{\pi} = 8.24\text{V}$$

The peak inverse voltage is

$$\text{PIV} = V_m = 25.9\ \text{V}$$

6.3.3 Full-wave Rectification

In a half-wave rectifier, discussed above, we utilize only one half-cycle of the input wave. In a full-wave rectifier we utilize both the half cycles. Alternate half cycles are inverted to give a unidirectional load current. There are two types of rectifier circuit that are in use. One is called centre-tap rectifier and uses two diodes. The other is called bridge rectifier and uses four diodes.

Centre-Tap Rectifier

The circuit of a centre-tap rectifier is shown in Fig.6.13a. It uses two diodes D1 and D2. During the positive half-cycles of secondary voltage, the diode D1 is forward biased and D2 is reverse biased. The current flows through the diode D1, load resistor R_L, and the upper half of the winding, as shown in Fig.6.13b. During negative half-cycles diode D2 becomes forward biased and D1 reverse biased. Now D2 conducts and D1 becomes open. The current flows through diode D2, load resistor R_L, and the lower half of the winding , as shown in Fig.6.13c. Note that the load current in both Figs. 6.13b and c is in the same direction. The waveform of the current i_L, and hence of the load voltage V_o, is shown in Fig.6.13d.

Peak Inverse Voltage

Fig.6.14 shows the centre-tap rectifier circuit at the instant the secondary voltage reaches its positive maximum value.

The voltage V_m is the maximum (peak) voltage across half of the secondary winding. At this instant, the diode D1 is conducting and it offers almost zero resistance. The whole of the voltage V_m across the upper half winding appears across the load resistor R_L. Therefore the reverse voltage that appears across the nonconducting diode is the summation of the

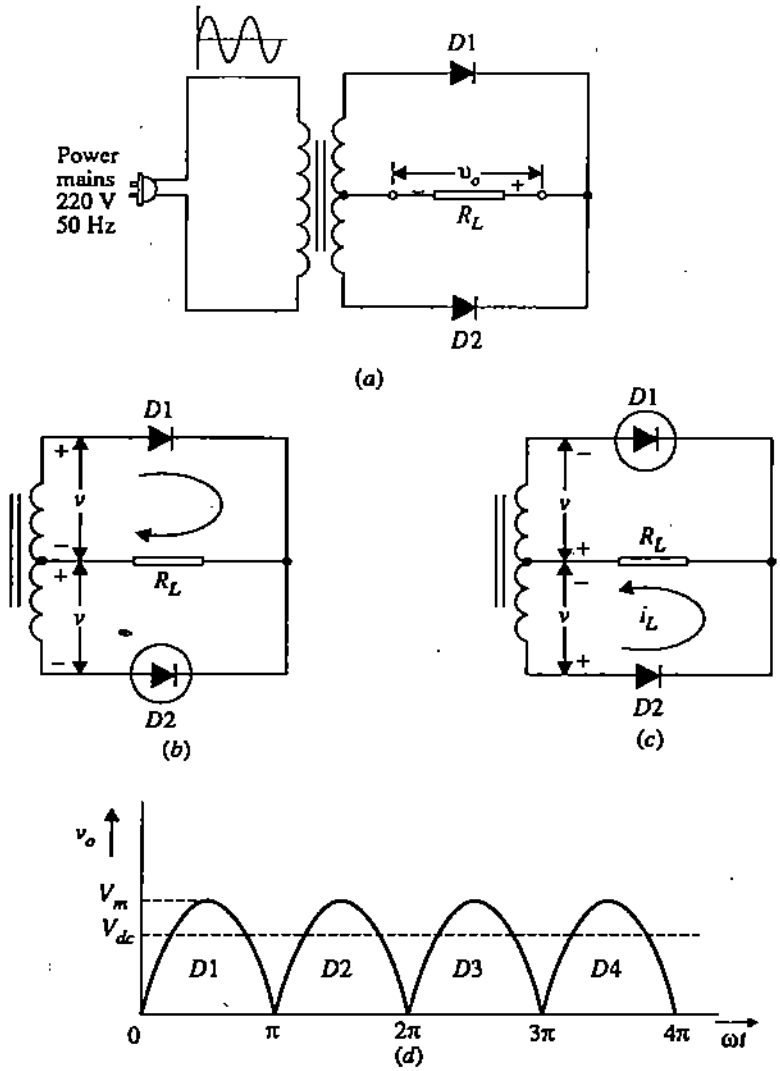


Fig.6.13: Centre-tap full-wave rectifier.

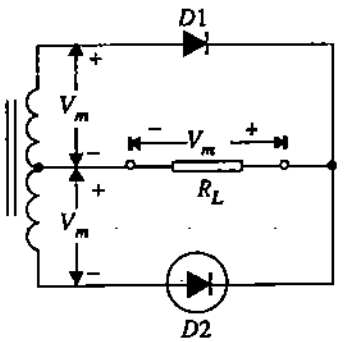


Fig.6.14: The PIV across the non-conducting diode D2 in a centre-tap rectifier is $2V_m$.

voltage across the lower half winding and the voltage across the load resistor R_L. From the figure this voltage is $V_m + V_m = 2V_m$. Thus,

$$\text{PIV} = 2V_m \qquad (6.12)$$

Bridge Rectifier

A more widely used full-wave rectifier circuit is the bridge rectifier, shown in Fig.6.15a. It requires four diodes instead of two, but avoids the needs for a centre-tapped transformer. During the positive half-cycle of the secondary voltage, diodes D2 and D4 are conducting and diodes D1 and D3 are nonconducting. Therefore, current flows through the secondary winding, diode D2 load resistor R_L and diode D4, as shown in Fig.6.15b. During negative half-cycles of the secondary voltage, diodes D1 and D3 conduct, and the diodes D2 and D4

do not conduct. The current flows through the secondary winding, diode D1, load resistor R_L and diode D3, as shown in Fig.6.15c. In both cases, the current passes through the load resistor in the same direction. Therefore, a fluctuating, unidirectional voltage is developed across the load. The load voltage waveform is shown in Fig.6.15d.

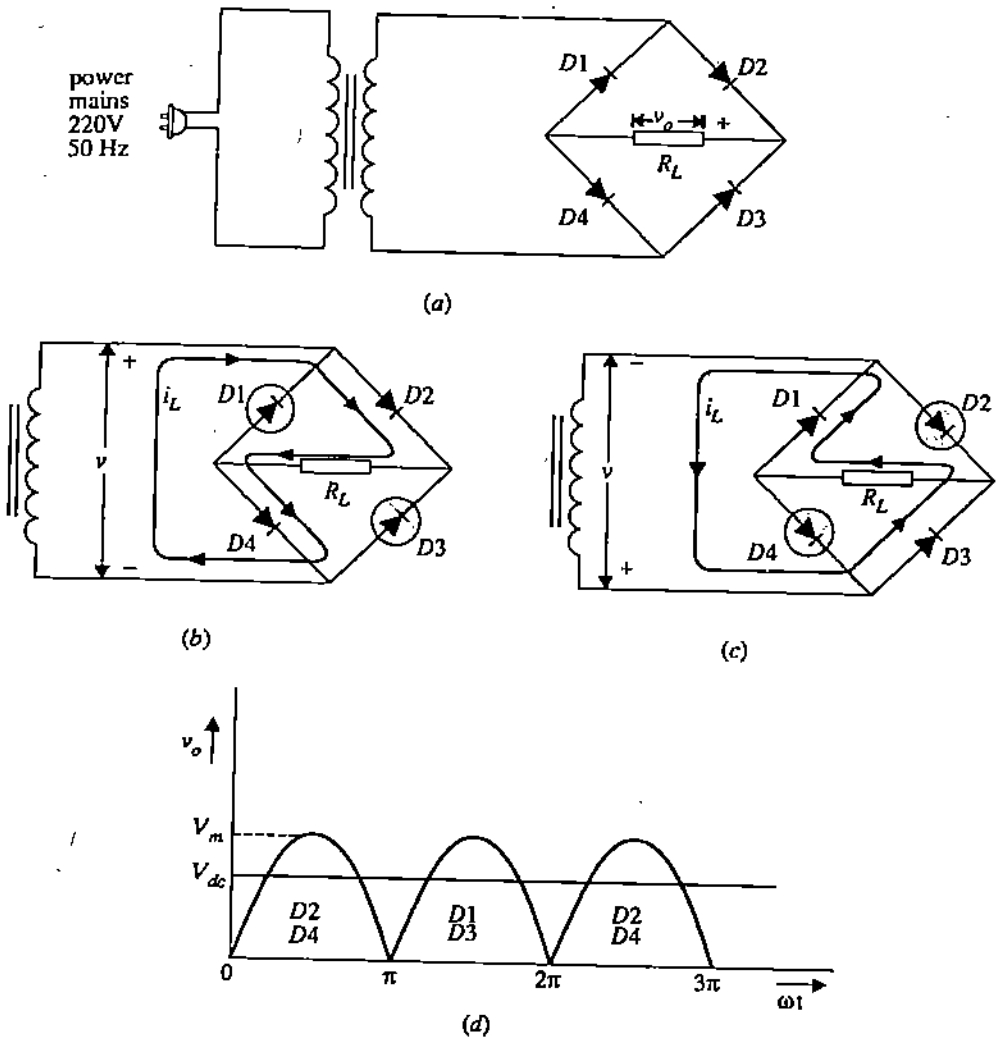


Fig.6.15: Bridge rectifier.

Peak Inverse Voltage

Let us now find the peak inverse voltage that apears across a nonconducting diode in a bridge rectifier. Fig.6.16 shows the bridge rectifier circuit at the instant the secondary voltage reaches its positive peak value, V_m. The diodes D2 and D4 are conducting, whereas diodes D1 and D3 are reverse biased and are nonconducting. The conducting diodes D2 and D4 have almost zero resistance (and hence zero voltage drops across them). Point B is at the same potential as the point A. Similarly, point D is at the same potential as the point C. The entire voltage V_m across the secondary winding appears across the load resistor R_L. The reverse voltage across the nonconducting diode D1 (or D3) is also V_m. Thus,

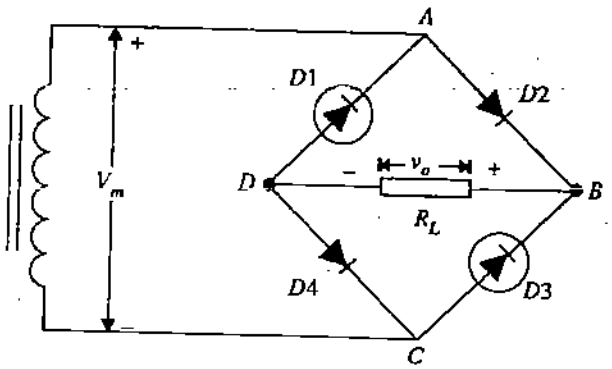


Fig.6.16: The PIV across the nonconducting diode D1 or D3 is V_m.

$$PIV = V_m \tag{6.13}$$

Output dc Voltage in Full Wave Rectifiers

The voltage waveform in Fig.6.15d is exactly the same as that in Fig.6.13d. In both the rectifier circuits, the load voltage is the same. However, there is one difference. In the bridge rectifier, V_m is the maximum voltage across the secondary winding. But in the centre-tap rectifier, V_m represents the maximum voltage across half the secondary winding.

Now let us compare the full-wave rectified voltage waveform (of Fig.6.15d or Fig.6.13d) with the half-wave rectified voltage waveform (of Fig.6.9b). In a half-wave rectifier, only positive half-cycles are utilized for the dc output. But a full-wave rectifier utilizes both the half-cycles. There, the dc or average voltage available in a full-wave rectifier will be double the dc voltage available in a half-wave rectifier. If the resistance of a forward biased diode is assumed zero, the dc voltage of a full-wave rectifier (refer Eq.6.11) is

$$V_{dc} = \frac{2V_m}{\pi} \tag{6.14}$$

We can mathematically derive Eq.6.14. on the same lines as we derived Eq. (6.8) in the previous sub-section. Try to derive it by solving the following SAQ.

SAQ 3

The output voltage of a full wave rectifier (see Fig.6,15b) is described as :

$$V_o = V_m \sin \omega t \qquad 0 < \omega t < \pi$$

$$V_o = -V_m \sin \omega t \qquad \pi < \omega t < 2\pi$$

A minus sign appears in the second equation because during the second half-cycle the wave is still sinusoidal, but inverted. The average or the dc value of voltage is

$$V_{dc} = \frac{1}{2\pi} \int_0^{2\pi} V_o \, d(\omega t)$$

Prove that

$$V_{dc} = \frac{2V_m}{\pi}.$$

Therefore, a dc power unit can take one of the three forms: it can contain a half-wave rectifier, or a full-wave rectifier or a bridge rectifier circuit.

You have seen that the types of rectifiers described above convert an a-c input into a fluctuating d-c output. The fluctuation of the d-c output above and below its average value is called ripple. In a half-wave rectifier, the frequency of the ripple is the same as the frequency of the a-c input, because it produces one pulse per cycle. In a full-wave rectifier, the ripple frequency is twice that of the a-c input, because two pulses per cycle are produced.

Most electronic equipment requires smooth d-c operating voltages. The output of a rectifier cannot be applied directly to such equipment because of the ripple. Consequently, the ripple must be eliminated. Circuits for accomplishing this are called filter circuits. But before studying about filter circuits let us know what does riple factor, rectifier efficiency mean.

6.4 HOW EFFECTIVELY A RECTIFIER CONVERTS ac INTO dc

If we connect a load resistor R_L directly across an ac power mains, the current flowing through it will be purely ac (sinusoidal having zero average value). This current is shown in Fig.6.17a.

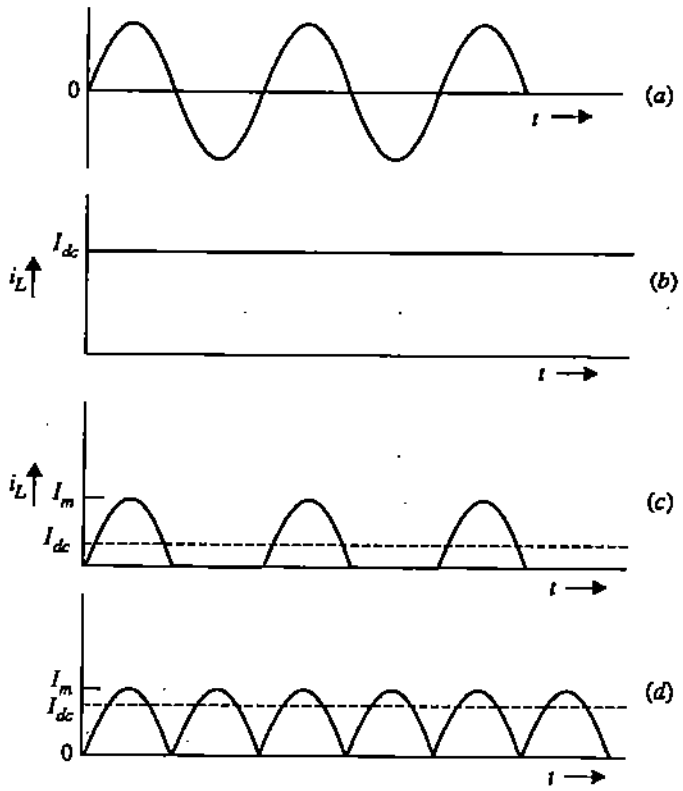


Fig.6.17: Comparison of half-wave and full-wave rectifiers with an ideal ac-to-dc converter.

In some applications, we require a dc current to flow through the load. The dc current is unidirectional and, ideally, has no fluctuations with time. The ideal dc current is shown in Fig.6.17b. To see how effectively a rectifier converts ac into dc, we compare its output current waveshape with the ideal dc current.

If the load takes current from a half-wave rectifier, the current waveform will be as in Fig.6.17c. It is unidirectional, but fluctuates greatly with time. The waveform of the load current, when the load is connected to a full-wave rectifier, is shown in Fig.6.17d. This too is unidirectional and fluctuates with time. A unidirectional, fluctuating waveform may be considered as consisting of a number of components. It has an average or dc value over which are superimposed a number of ac (sinusoidal) components of different frequencies. These undesired ac components are called ripples. The lowest ripple frequency in case of a half-wave rectifier is the same as the power-mains frequency. But, for full-wave rectifier it is not so. As can be seen from Figs.6.17d and a, the period of the output wave of a full-wave rectifier is half the period of the input wave. The variation in current (or voltage) repeats itself after each angle π of the input wave. Therefore, the lowest frequency of the ripple in the output of a full-wave rectifier is twice the input frequency. That is, the ripple frequency

$$f_r = f_i = 50 \text{ Hz} \quad \text{(half-wave rectifier)} \tag{6.15}$$

and

$$f_r = 2f_i = 100 \text{ Hz} \qquad \text{(full-wave rectifier)} \tag{6.16}$$

How effectively a rectifier converts ac power into dc power is described quantitatively by terms such as ripple factor, rectification efficiency, etc.

The ripple factor is a measure of purity of the dc output of a rectifier, and is defined as

$$r = \frac{\text{rms value of the components of wave}}{\text{average or dc value}} \tag{6.17}$$

The rectification efficiency tells us what percentage of total input ac power is converted into useful dc output power. Thus, rectification efficiency is defined as

$$\eta = \frac{\text{dc power delivered to load}}{\text{ac input power from transformer secondary}}$$

or $$\eta = \frac{P_{dc}}{P_{ac}} \tag{6.18}$$

Here, P_{ac} is the power that would be indicated by a wattmeter connected in the rectifying circuit with its voltage terminals placed across the secondary winding and P_{dc} is the dc output power.

We shall now analyse half-wave and full-wave rectifiers to find their ripple factor and rectification efficiency.

6.4.1 Performance of Half-wave Rectifier

The half-wave rectified current wave is plotted in Fig.6.18 and is described mathematically as

$$i_L = I_m \sin \omega t ; \quad \text{for } 0 < \omega t < \pi \tag{6.19}$$

and

$$i_L = 0 ; \quad \text{for } \pi < \omega t < 2\pi \tag{6.20}$$

For determining the ripple factor or rectification efficiency, we first find the rms value of the current.

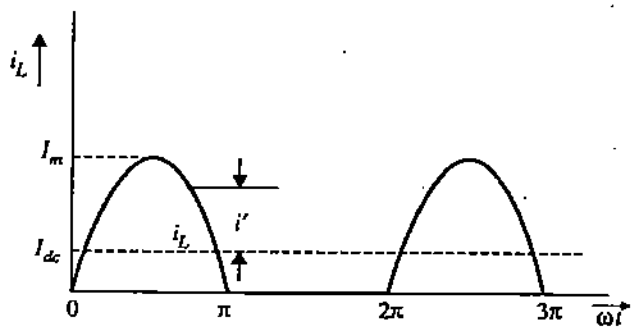


Fig.6.18: Half-wave rectified current waveform. (The instantaneous ac component of current is the difference between instantaneous total current and dc current, i.e., $i' = i_L - I_{dc}$.)

RMS Value of Current

The rms or effective value of the current flowing through the load is given as

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 (\omega t)}$$

where current i_L is described by Eqs. (6.19) and (6.20). Therefore,

$$I_{rms} = \sqrt{\frac{1}{2\pi}\left[\int_0^{\pi} I_m^2 \sin^2 \omega t \, d(\omega t) + \int_{\pi}^{2\pi} 0 \, d(\omega t)\right]}$$

$$= \frac{I_m^2}{2\pi}\int_0^{\pi} \frac{(1 - \cos 2\omega t)}{2} d(\omega t)$$

$$= \sqrt{\frac{I_m^2}{2\pi \times 2}\left|\omega t - \frac{\sin 2\omega t}{2}\right|_0^{\pi}}$$

or

$$I_{rms} = \frac{I_m}{2} \tag{6.21}$$

This is the rms value of the total current (dc value and ac components). As can be seen from Fig.6.18, the instantaneous value of ac fluctuation is the difference of the instantaneous total value and the dc value. That is, the instantaneous ac value is given as

$$i' = i_L - I_{dc}$$

Therefore, the rms value of ac components is given as

$$I'_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}(i_L - I_{dc})^2\, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(i_L^2 + I_{dc}^2 - 2i_L I_{dc}\right) d(\omega t)}$$

$$= \sqrt{I_{rms}^2 + I_{dc}^2 - 2I_{dc}^2}$$

or $$I'_{rms} = I_{rms} - I_{dc} \qquad (6.22)$$

Ripple Factor

From Eq. 6.17, the ripple factor is given as

$$r = \frac{I'_{rms}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \qquad (6.23)$$

Using Eqs. 6.8 and 6.21, fo half-wave rectifier the ratio

$$\frac{I_{rms}}{I_{dc}} = \frac{I_m/2}{I_m/\pi} = 1.57$$

Therefore, the ripple factor is given as

$$r = \sqrt{(1.57)^2 - 1} = 1.21 \qquad (6.24)$$

Thus, we see that the ripple current (or voltage) exceeds the dc current (or voltage). This shows that a half-wave rectifier is a poor converter of ac into dc.

Rectification Efficiency

For a half-wave rectifier, the dc power delivered to the load is

$$P_{dc} = I_{dc}^2 R_L = \left(\frac{I_m}{\pi}\right)^2 R_L$$

and the total input ac power is

$$P_{ac} = I_{rms}^2 (r_d + R_L) = \left(\frac{I_m}{2}\right)^2 (r_d + R_L)$$

Therefore, the rectification efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(I_m/\pi)^2 R_L}{(I_m/2)^2 (r_d + R_L)} \times 100\%$$

$$= \frac{40.6}{1 + r_d/R_L}\% \qquad (6.25)$$

If $r_d < R_L$, $\eta \to 40.6$ per cent. It means that under the best conditions (i.e. no diode loss), only 40.6% of the ac input power is converted into dc power. The rest remains as ac power in the load.

6.4.2 Performance of Full-wave Rectifier

Fig.6.19 shows a full-wave rectified current waveform. Its period may be seen to be π. The wave repeats itself after each π. Therefore, while computing the average or rms values, we should take the integration between the limits 0 to π, instead of 0 to 2π. The waveshape between is described as

$$i_L = I_m \sin \omega t \qquad (6.26)$$

where ω ($= 2\pi f$) is the angular frequency of the input ac voltage.

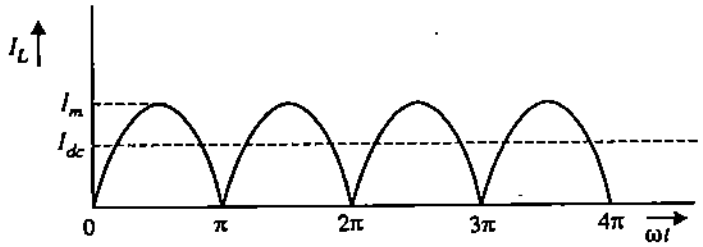


Fig.6.19: Full-wave rectified current waveform.

RMS Value of Current

Effective or rms value of current is given as

$$I_{rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L^2\, d(t)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m^2 \sin^2 \omega t\, d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right) d(\omega t)} = \sqrt{\frac{I_m^2}{\pi}\left|\frac{\omega t}{2} - \frac{\sin 2\omega t}{4}\right|_0^{\pi}}$$

$$= \sqrt{\frac{I_m^2}{\pi} \times \frac{\pi}{2}}$$

or

$$I_{rms} = \frac{I_m}{\sqrt{2}} \tag{6.27}$$

Note that this is the same as the rms value of the full sinusoidal ac wave.

The dc or average value of the current is

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} i_L\, d(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_m \sin \omega t\, d(\omega t)$$

$$= \frac{2 I_m}{\pi} \tag{6.28}$$

This current, as it should be, is double the dc current of a half-wave rectifier.

Ripple Factor

Eq.(6.22) is valid for a full-wave rectifier too. We can therefore use Eq. 6.23 to calculate the ripple factor of a full-wave rectifier.

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \left(\frac{I_m/\sqrt{2}}{2 I_m/\pi}\right)^2 - 1$$

$$= 0.482 \tag{6.29}$$

Rectification Efficiency

For a full-wave rectifier, the dc power delivered to the load is

$$P_{dc} = I_{dc}^2 R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

and the total input ac power is

$$P_{ac} = I_{rms}^2 (r_d + R_L) = \left(\frac{I_m}{\sqrt{2}}\right)^2 (r_d + R_L)$$

Therefore, the rectification efficiency is

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 R_L}{(I_m\sqrt{2})^2 (r_d + R_L)} \times 100\%$$

$$= \frac{81.2}{1 + r_d/R_L}\% \qquad (6.30)$$

This shows that the rectification efficiency of a full wave rectifier is twice that of a half-wave rectifier under identical conditions. The maximum possible efficiency can be 81.2% (when $r_d < R_L$).

Example 2

In a centre-tap full-wave rectifier, the load resistance $R_L = 1\ \text{k}\Omega$. Each diode has a forward-bias dynamic resistance r_d of $10\ \Omega$. The voltage across half the secondary winding is $220 \sin 314t$. Find (a) the peak value of current, (b) the dc or average value of current, (c) the rms value of current, (d) the ripple factor, and (e) the rectification efficiency.

Solution

The voltage across half the secondary winding is given as

$$v = 220 \sin 314\, t$$

(a) The peak value of voltage is

$$V_m = 220\text{V}$$

Therefore, peak value of current is

$$I_m = \frac{V_m}{r_d + R_L} = \frac{220}{10 + 1000} = 0.2178\text{A}$$

$$= 217.8\ \text{mA}$$

(b) The dc or average value of current is

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2 \times 217.8}{\pi} = 138.66\ \text{mA}$$

(c) The rms value of current is

$$I_{rms} = \frac{I_m}{\sqrt{2}} = 154\ \text{mA}$$

(d) The ripple factor is given as

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \qquad = \sqrt{\left(\frac{154}{138.66}\right)^2 - 1} = 0.482$$

(e) The rectification efficiency is given as

$$\eta = \frac{P_{dc}}{P_{ac}}$$

But, $P_{dc} = I_{dc} R_L = (1.38.66)^2 \times (10^{-3})^2 \times 1000 = 19.2265\ \text{W}$

$$\therefore \eta = \frac{P_{dc}}{P_{ac}} = \frac{19.2265}{23.953} = 0.8026 \times 100\% = 80.26\%$$

A full-wave rectifier is preferred to a half-wave rectifier, because its rectification efficiency is double and its ripple factor is low. Table 6.1 gives the comparison between different rectifiers discussed so far. Unless otherwise indicated, all rectifiers discussed from now on are full-wave rectifiers (either centre-tap or bridge).

Table 6.1: Comparison Between Different Rectifiers.

	Half-wave	Full-wave	
		Centre-tap	Bridge
Number of diodes	1	2	4
Transformer necessary	No	Yes	No
Peak secondary voltage	V_m	V_m	V_m
Peak inverse voltage	V_m	$2V_m$	V_m
Peak load current, I_m	$V_m/(r_d+R_L)$	$V_m/(2r_d+R_L)$	$V_m/(2r_d+R_L)$
RMS current, I_{rms}	$I_m/2$	$I_m/2$	$I_m/2$
DC current, I_{dc}	I_m/π	$2I_m/\pi$	$2I_m/\pi$
Ripple factor, r	1.21	0.482	0.482
Rectification efficiency (max)	40.6%	81.2%	81.2%
Lowest ripple frequency, f_i	f_i	$2f_i$	$2f_i$

6.5 FILTER CIRCUITS

The object of rectification is to provide a steady dc voltage, similar to the voltage from a battery. We have seen that a full-wave rectifier provides a better dc than a half-wave rectifier. But, even a full-wave rectifier does not provide ripple-free dc voltage. The rectifiers provide what we may call "a pulsating dc". We can filter or smooth out the ac variations from the rectified voltage. For this we use a filter or smoothing circuit (see Fig.6.1). In this section, we shall discuss different types of filter circuits.

6.5.1 Capacitance Filter

The ripple output of a rectifier represents energy being supplied to the load in pulses. The ripple fluctuations can be reduced considerably if some of the output is stored while the rectifier is delivering a pulse and then released to the load between output pulses. This is the basic operating principle of the capacitance filter.

Such a filter consists of a large value capacitor C in shunt with the load resistor R_L, as shown in Fig.6.20a. The capacitance offers a low-resistance path to the ac components of current. To dc (with zero frequency), this is an open circuit. All the dc current passes through the load. Only a small part of the ac component passes through the load producing a small ripple voltage.

The capacitor changes the conditions under which the diodes (of the rectifier) conduct. When the rectifier output voltage is increasing, the capacitor charges to the peak voltage V_m. Just past the positive peak, the rectifier output voltage tries to fall (see the dotted curve in Fig.6.20b). But at point B, the capacitor has + V_m volts across it. Since the source voltage becomes slightly less than V_m the capacitor will try to send current back through the diode (of the rectifier). This reverse-biases the diode, i.e. it becomes open-circuited.

The diode (open-circuit) disconnects or separates the source from the load. The capacitor starts to discharge through the load. This prevents the load voltage from falling to zero. The capacitor continues to discharge until the source voltage (the dotted curve) becomes more than the capacitor voltage (at point C). The diode again starts conducting, and the capacitor is again charged to peak value V_m. During the time the capacitor is charging (from point C to point D) the rectifier supplies the charging current i_c through the capacitor branch as well as the load current i_L. When the capacitor discharges (from point B to point C), the rectifier does not supply any current, the capacitor sends current i_L through the load. The current is maintained through the load all the time.

The rate at which the capacitor discharges between points B and C (in Fig.6.20) depends upon the time constant CR_L. The longer this time constant is, the steadier is the output voltage. If the load current is fairly small (i.e., R_L is sufficiently large) the capacitor does not discharge very much, and the average load voltage V_{dc} is slightly less than the peak value V_m (see Fig.6.20b).

Any increase in the load current (i.e. decrease in the value of R_L) makes the time constant of the discharge path smaller. The capacitor then discharges more rapidly, and the load voltage is not constant (see Fig.6.20c). The ripple increases with increase in load current. Also, the dc output voltage, V_{dc} decreases.

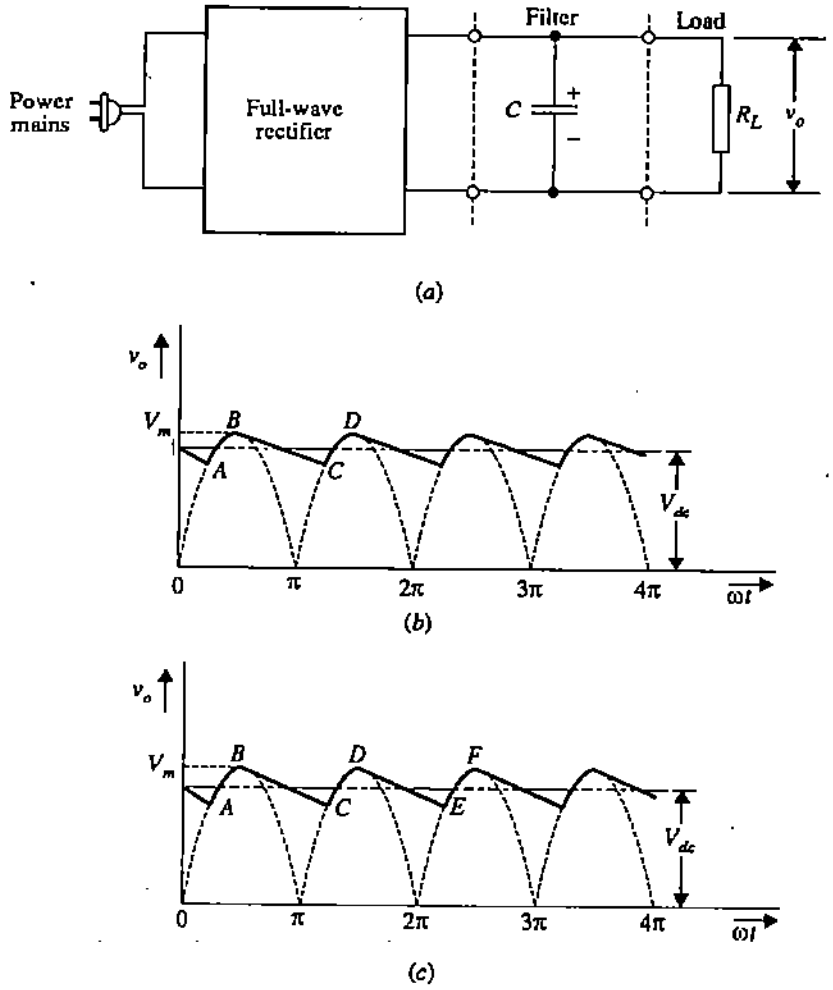


Fig.6.20 : Full-wave rectifier with shunt capacitance filter.

6.5.2 Inductance Filter

An inductor is another device that can alternately store and release electrical energy. It does this by extracting energy from a flowing current and storing it in a magnetic field when the current is increasing. Then it releases the energy to keep the current flowing when the current begins to decrease. This ability of an inductor to store and release energy can be used to help prevent the abrupt changes in the output of a rectifier. This property is used in the inductance filter of Fig.6.21. Whenever the current through an inductor tends to change, a "back emf" is induced in the inductor. This induced back emf prevents the current from changing its value. Any sudden change in current that might have occurred in the circuit without an inductor is smoothed out by the presence of the inductor. Its effects on the output waveform is shown in Fig.6.21b.

The inductance filter prevents the current, and, therefore, the output voltage from ever reaching the peak value that would be obtained if the inductor were not in the circuit.

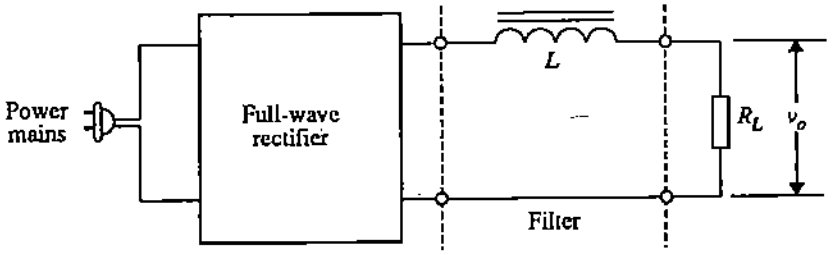


Fig.6.21: Full-wave rectifier with inductance filter.

Therefore, a rectifier that has an inductance filter will not produce as high an output voltage as one that has a capacitance filter. However, a large load current can be drawn from the inductance filter without changing the output voltage.

The operation of a series inductor filter depends upon the current flowing through it. Therefore this filter (and also the choke-input LC filter discussed in the next sub-section) can only be used together with a full-wave rectifier (since it requires current to flow at all times). Furthermore, the higher the current flowing through it, the better is its filtering action. Therefore, an increase in load current results in reduced ripple.

6.5.3 LC Filter

We have seen that an inductance filter has a feature of decreasing the ripples when the load current is increased. Reverse is the case with a capacitor filter. In this case, as the load current is increased, the ripples also increase. An LC filter combines the features of both the inductor filter and shunt capacitor filter. Therefore, the ripples remain fairly the same even when the load current changes. There are two types of LC filter: capacitor input filter and Choke input filter. Let us describe each one of them.

Capacitor input filter

This type of LC filter is shown in Fig.6.22. This is called the capacitor input filter because capacitor (C_1) is the first filtering element directly after the rectifier. It is also called the "pi" filter because of its schematic resemblence to the Greek letter π.

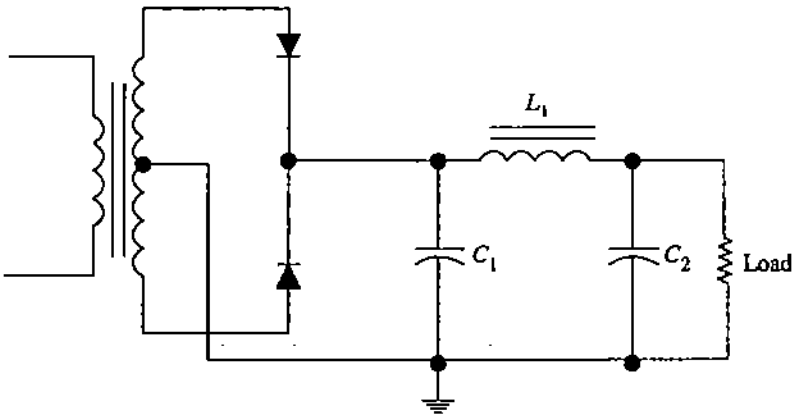


Fig.6.22: Capacitor input filter.

In this type of filter, capacitor C_1 performs the same function as the simple capacitor filter previously described. It charges on the peaks of the rectified output pulses and then discharges through the load, when the rectifier output falls. Capacitor C_2 provides similar filtering action but to a lesser degree. Inductor L_1 adds to the overall filtering action by opposing changes in both the output current filtered by C_2 and the current drawn by the load.

The output of such a filter contains only small amount of ripple. However, the voltage regulation of such a filter is relatively poor. This is because of the decrease in the voltage across C_1 as it discharges between rectified pulses.

Choke input filter

When an inductor is used as primary filtering element in an LC filter, the network is called a choke input filter. The term choke is used because of the inductor's ability to stop, or choke, the passage of ripple voltage to the load. Fig.6.23 shows a simple choke input filter.

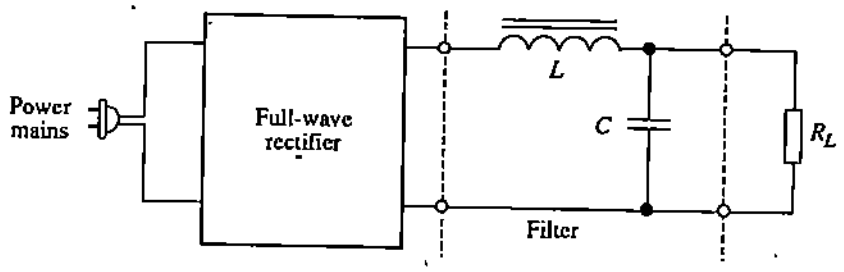


Fig.6.23: Choke input filter.

The inductor opposes current changes while the capacitor charges and discharges in standard filter-capacitor fashion. Since the inductor reduces the peak rectifier current and this inturn reduces the maximum voltage to which the capacitor charges, the output voltage of the choke input filter is lower than that of the capacitor input filter. This output voltage, though, is affected less by changes in the load current.

6.6 REGULATION OF OUTPUT VOLTAGE

In the previous section we have discussed the filter system. The filters are used to reduce the ripple and help in regulation of voltage. A very important characteristic of any power supply is the degree to which its output voltage remains constant despite changes in the amount of current drawn from the supply by the load. This characteristic is called the **regulation** of the supply. A supply whose output voltage changes little over a wide variation in load current is said to have good regulation. One whose output voltage falls sharply as the load current increases has poor regulation. Certain types of power supplies have inherently good regulation, mainly because of the type of filter used. However, for many applications, even these supplies do not have good regulation. Additional circuits are added so that the output voltage remain constant. These additional circuits are called voltage regular circuits.

Basically, the output voltage tends to vary because of two things : (1) fluctuating line voltage and (2) fluctuating load current. Every time the line voltage goes up, the output voltage will go up. But when the load current goes up, the output voltage will go down. This is because the output voltage is actually what is left after the internal voltage drops of the supply are taken away from the output. As the load increases, the internal drop increases and less is left for the output. Thus we define two terms: (i) source regulation and (ii) load regulation.

Source regulation: It is also called source effect or line regulation. It is the change in regulated load voltage for the specified range of line voltage and is defined as:

$$\%SR = \frac{SR}{V_{nom}} \times 100\%$$

where

$\%SR$ = percent source regulation

SR = change in load voltage for full line change

V_{nom} = nominal load voltage .

For instance, if the change in load voltage is 5mV and the nominal load voltage is 10V then

$$\% \text{ source regulation} = \frac{5\text{mV}}{10\text{V}} \times 100\% = 0.05\%$$

Load regulation: It is also called load effect. It is defined as the change in regulated output voltage when the load current changes from minimum to maximum

$$LR = V_{NL} - V_{FL}$$

where LR = load regulation

V_{NL} = load voltage with no load current

V_{FL} = load voltage with full load current

Load regulation is often expressed as a percent by dividing the change in load voltage by the no load voltage.

$$\%LR = \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100\%$$

where $\%LR$ = percent load regulation

V_{NL} = load voltage with no load current

V_{FL} = load voltage with full load current

For instance, if no load voltage is 10V and the full load voltage is 9.9V, then the percent load regulation is

$$\%LR = \frac{10V - 9.9V}{10V} \times 100\% = 1\%$$

6.6.1 Principal of Regulation

The basic regulator circuit works by inserting resistance in the output of the supply. When a load resistor is connected across the filter circuit it provides a small degree of regulation. Let us understand how it works. Fig.6.24 shows that a load resistor and the load are connected directly across the power supply output. When either the load current increases or the ac input voltage decreases, the supply output voltage and therefore the voltage across R, tend to decrease. This means that less current-flows through R in accordance with Ohm's law. As a result, the portion of the internal voltage drop in the supply caused by R goes down somewhat to increase the output voltage by the same amount.

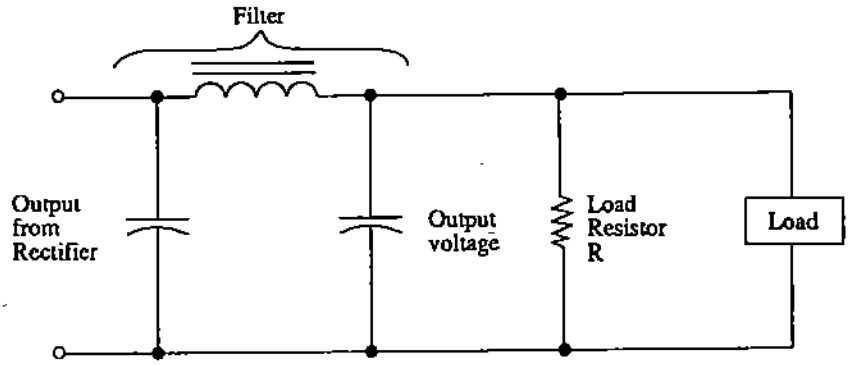


Fig.6.24: The load resistor provides a small degree of voltage regulation.

The opposite situation occurs if the output voltage tends to increase. The resulting higher voltage causes more current to flow through the load resistor, which increases the internal voltage drops of the supply so that the output voltage goes down.

.f the load resistor is replaced by a device that would cause large changes in internal voltage drops for small change in output voltage, much better regulation could be obtained. Such a device should have non-linear characteristic instead of following Ohm's law. Such a device is zener diode.

6.6.2 Zener Regulator

Fig.6.25 shows the simplest regulator circuit consisting of a resistor R_S connected in series with the input voltage and a zener diode connected in parallel with the load. The voltage from the dc power unit is used as the input voltage V_1 to the regulator circuit. The zener diode is reverse biased so that it operates in break down region. Furthermore, to produce break down, the voltage across R_L should be greater than the zener breakdown voltage V_Z. A series resistor is always used to limit the zener current to less than its current rating otherwise, the zener diode will burn out with too much power dissipation.

The current from the dc power unit splits at the junction of the zener diode and the load resistor.

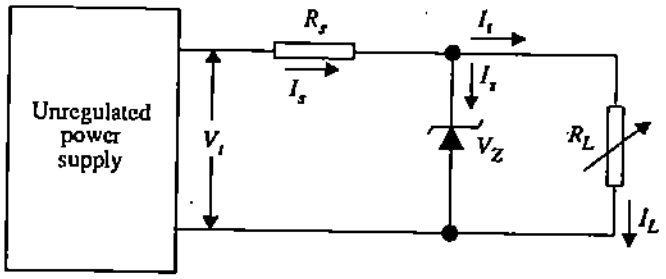


Fig.6.25: Simplest regulator circuit.

Therefore,

$$I_S = I_Z + I_L \tag{6.31}$$

When the zener diode operates in its breakdown region, the voltage V_Z across it remains fairly constant even though the current I_Z flowing through it may vary considerably. If the load current I_Z increases (because of reduction in load resistance), the current I_Z through the zener diode will decrease in order to maintain constant current I_S. This keeps the voltage drop across R_S constant. Hence the output voltage V_o goes upto normal. If on the other hand, the load current decreases, the zener diode passes an extra current I_Z such that I_S is kept constant. Thus, the output voltage of the circuit is stabilized.

Let us examine the other cause of the output voltage variation. If the input voltage V_I increases, there is more current through the zener diode but at the same zener voltage. This is the basic idea of voltage regulation.

6.7 SUMMARY

- d.c. power unit converts the a.c. mains into one or more dc voltages with relatively poor regulation and significant ripple voltage superimposed on the dc output voltage.
- The ac mains voltage is first reduced by means of a transformer. With an untapped secondary winding the ac is rectified either by a half-wave rectifier circuit or by a bridge circuit. With a centre-tapped secondary winding, ac is rectified by a full-wave rectifier circuit.
- A half-wave rectifier consists of a diode and a load resistor. It delivers an output during only half of the input voltage cycle,
- Full-wave rectifier circuit consists of two diodes having a common load. It delivers an output during both halves of the input voltage cycle.
- Bridge rectifier consists of four diodes and a common load. The output voltage produced by it is nearly twice as large as that produced by full-wave rectifier.
- Fluctuation of the dc output from a rectifier above and below its average value is called ripple.
- Capacitor filter consists of a capacitor connected across the rectifier output.
- Inductance filter consists of an inductor connector in series with the rectifier load.

6.8 TERMINAL QUESTIONS

1. If the peak voltage across a transformer secondary is 100 volts, what is the peak value of a half wave rectified voltage ? Full Wave ? Bridge ?
2. Which has greater ripple frequency: a half wave rectifier whose input is 500 cps, or a full wave rectifier whose input is 300 cps ?
3. The turns ratio of the transformer used in a bridge rectifier is $n_1 : n_2 = 12 : 1$. The primary is connected to 220 V, 50 Hz power mains. Assuming that the diode voltage drops to be zero, find the dc voltage across the load. What is the PIV of each diode ? If the same dc voltage is obtained by using a centre tap rectifier, what is the PIV ?

4. In a full-wave rectifier without filter, the load resistance is of 400 ohms. Each diode has a resistance of 800 ohms, voltage applied to each diode is 240 sin 100 πt. Calculate

   a) peak, average and r.m.s. values of current,

   b) dc power output and total power input

   c) rectifier efficiency

   d) form factor

   e) ripple factor

6.9 SOLUTIONS & ANSWERS

SAQs

1. a) The r.m.s. value of a sinusoidal waveform is the amplitude divided by $\sqrt{2}$, so in this case the amplitude, or maximum voltage, is $220 \times \sqrt{2} = 311$ V.

   b) Maximum voltage across primary $= 220 \times \sqrt{2} = 311$ V.

   Maximum voltage across secondary $= \frac{311}{16} = 20.7$ V.

2. The difference between the output voltage and input voltage is caused by the presence of a silicon (or Germanium diode). When the transformer output voltage is positive the diode conducts, so the voltage applied to the load resistance is the ac voltage minus the voltage dropped across the diode. When the transformer output voltage is negative no current flows so there is zero voltage drop across the load, as shown.

3.
$$V_{dc} = \frac{1}{2\pi}\int_{o}^{2\pi} v_o \, d(\omega t)$$

$$= \frac{1}{2\pi}\int_{0}^{\pi} (V_m \sin\omega t \, d(\omega t) + \int_{\pi}^{2\pi} (-V_m \sin\omega t) \, d(\omega t)$$

$$= \frac{1}{2\pi}\left[|-V_m \cos\omega t|_0^{\pi} + |V_m \cos\omega t|_{\pi}^{2\pi} \right]$$

$$= \frac{V_m}{2\pi}\left[-\cos\pi + \cos 0 + \cos 2\pi - \cos\pi \right]$$

$$= \frac{2V_m}{\pi}.$$

This is same as Eq. 6.12.

TQs

1. $\frac{100}{\pi}$ volts, $\frac{200}{\pi}$ volts, $\frac{200}{\pi}$ volts

2. Full-wave rectifier.

   For half-wave rectifier, ripple frequency is 500 cps.

For full-wave rectifier, ripple frequency is $300 \times 2 = 600$ cps.

3. The maximum primary voltage is

$$V_p = \sqrt{2}\, V_{rms} = \sqrt{2} \times 220 = 311\text{V}$$

Therefore, the maximum secondary voltage is

$$V_m = \frac{n_2}{n_1} V_p = \frac{1}{12} \times 311 = 25.9\text{V}$$

The dc voltage across the load is

$$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 25.9}{\pi} = 16.48\text{V}$$

The PIV (for bridge rectifier) is

$$\text{PIV} = V_m = 25.9\text{V}$$

For the centre-tap rectifier, the PIV is

$$\text{PIV} = 2V_m = 2 \times 25.9 = 51.8\text{V}$$

4. a) Peak value of current, $I_m = \frac{E_m}{r_d + R}$

$$\therefore I_m = \frac{240}{800 + 4000} = 50 \times 10^{-3}\text{A}$$

Average value of current, $I_{dc} = \frac{2I_m}{\pi} = \frac{50 \times 2}{3.14} = 31.84\text{ mA}$

The r.m.s. value of current output, $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{50}{1.41} = 35.36\text{ mA}$

b) The dc power output $P_{dc} = I_{dc}^2 \times R$

$$= (31.84)^2 \times 10^{-6} \times 4000$$

$$= 40.56\text{ watt.}$$

Total power input $P_{in} = (I_{rms})^2 \times (r_d + R)$

$$= (35.36 \times 10^{-3}A)^2 \times (800 + 4000)$$

$$6.0001\text{ watt}$$

c) Rectifier efficiency $\eta = \frac{P_{dc}}{P_{in}} = \frac{4.056}{6.001} \times 100\% = 67.59\%$

d) Form factor, $\frac{I_{rms}}{I_{dc}} = \frac{35.36}{31.84} = 1.11$

e) Ripple factor $= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

$$= \sqrt{(1.11^2) - 1} = 0.48$$

NOTES

NOTES

NOTES

Utter Pradesh
Rajarshi Tandon Open University

UGPHS-05
ELECTRICAL CIRCUITS AND ELECTRONICS

Block

3

LINEAR INTEGRATED CIRCUITS

BLOCK 3 LINEAR INTEGRATED CIRCUITS

In the previous two Blocks we dealt with electronic circuits and devices. In the present block, we will be studying about linear integrated circuits.

The linear integrated circuits is the most dominant technology in the present world of Electronics. With the advent of the transistor, the electronics engineers, were set to convert every thing that used vacuum tubes to solid state, the prime motivation was to reduce the size of electronic equipment, but not at the cost of reliability. Thus to improve the reliability and reduce the size and cost of electronic equipment gave birth to the linear integrated circuits. The first IC was manufactured by Texas Instruments in 1959. This circuit was an operational amplifier (OP amp). In Unit 7, we will study about the technical details, characteristics and functioning of the OP amps.

In Unit 8 we will study some of the important applications of OP amps. The use of an OP amp as inverting and non inverting amplifier will be dealt with. We will also learn how an OP amp can be used as an adder, differentiator and integrator.

In Unit 9 we will study about the special purpose I.C.s. The use of IC LM380 as a power amplifier in audio systems will be discussed. The 7800 and 7900 series or fixed positive and fixed negative voltage regulator ICS and LM317 and LM337 series of adjustable positive and negative voltage regulating ICs will be described.

UNIT 7 THE OPERATIONAL AMPLIFIER

Structure

7.1 INTRODUCTION

Operational Amplifier (Op Amp) was first designed in 1948 based upon a single vacuum tube. The primary use of early op amps was in analog computers. The op amps derived their first name 'operational' basically because at that time they were used in mathematical operations such as addition, subtraction, multiplication, division and solving differential equations.

The limited accuracy of analog computers upto three significant figures had limited their use. They were lather replaced by digital computers which were faster, more accurate and versatile.

With the advancement of integrated circuit (IC) technology, several types of IC based op amps were produced in mid-sixties which were available in the market. These op amps required much lower power as compared to the discrete components based amplifiers. They were cheaper and needed much less space. With such op amps commercially available, the task of designing circuits became very easy. With one or two op amps and a few resistors or some other components, very good quality amplifiers, signal generators, modulators, etc. could be made.

The sophistication in the recent times in the IC technology enabled the manufacturers to produce special purpose op amps. The dual and quad op amp packages have two

and four op amps respectively on a single chip. They are commercially available and are quite cheap.

For the user of an op amp it is not at all necessary to know the actual circuit of the operational amplifier which is grown on a single chip. The user neither derives any information from the circuit nor can change it. What the user needs is the performance characteristics of the op amp available in the data sheet supplied by the manufacturer. With such characteristics known, the user can use the op amp in any application where they fit in.

Objectives

After studying this unit, you should be able to :

- draw a schematic symbol for an op amp,
- distinguish between two types of packages of op amp IC,
- draw the pin-out diagram for op amp 741C,
- identify the manufacturer's name and temperature range of an op amp by noting the number code printed on the IC,
- explain the power supply requirements for op amps,
- state precautions which have to be borne in mind while working with op amps,
- establish input-output relationship for op amps,
- define input offset voltage, output offset voltage, differential input resistance, output resistance, common mode rejection ratio, maximum output current, power consumption, slew rate and gain bandwidth product,
- distinguish between the characteristics of ideal op amp and of 741C.
- describe the equivalent circuit of an op amp,
- draw the ideal voltage transfer curves for an op amp,
- describe comparators and zero crossing detector.

7.2 TECHNICAL DETAILS OF OP AMPS

Before learning the usage of op amp, we shall learn some general technical details of op amps and associated requirements in this section.

7.2.1 Symbol

The symbol used for op amp is shown in Fig.7.1. It is a triangle pointing to the signal flow. This symbol also shows part identification numbers (PIN) for a general

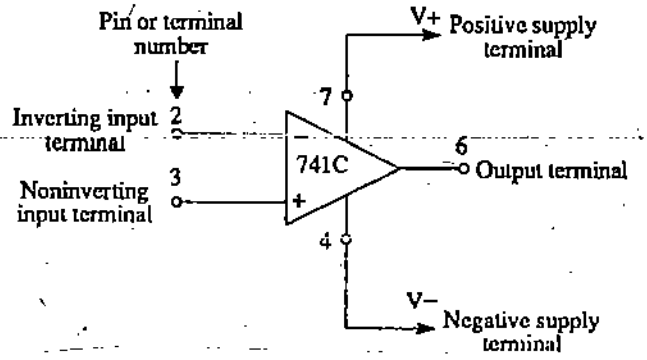


Fig.7.1: Circuit symbol for an op amp.

purpose and very popular op amp 741C. All op amps have at least five terminals—two for inputs, two for power supply and one for the output. General purpose 741C has other terminals as well.

The op amp input has two terminals. Pin 2 is named inverting input because when the input is given to it, the output at pin 6 is available with 180 degree phase change. Pin 3 is named non-inverting input because when the input is given to it, the output at pin 6 is available without phase change. Therefore, pin 2 is quite often shown with a (–) sign and non-inverting input with a (+) sign. These (–) and (+) terminals are quite often known as differential input terminals. The output voltage depends upon the difference in voltages between them.

Negative voltage terminal of the dual power supply is connected to pin 4 and positive voltage terminal is connected to pin 7. Note that if the polarities of the voltages applied to pins 4 and 7 are reversed the op amp shall be damaged and cannot be used.

SAQ 1

What are the numbers of input and output pins?

7.2.2 Package

The op amp which is fabricated on a silicon chip is housed in a suitable package. Op amp 741C is available in two most popular packages (a) metal can and (b) dual-in-line packages (DIP). These packages are shown in Fig.7.2 (a) and (b) respectively. The combination of the op amp symbol and package view is quite commonly used by the manufacturers in their data sheets. These combinations are shown in Fig.7.3 (a) and (b) respectively.

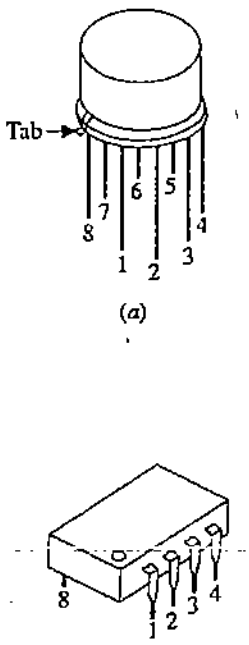
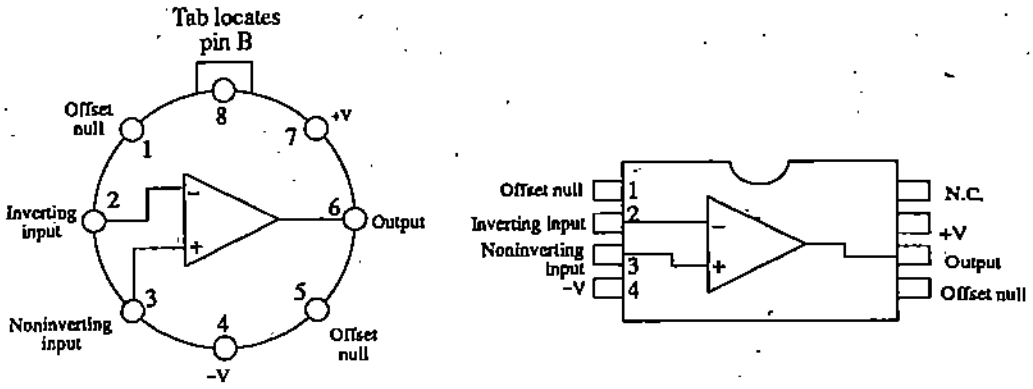


Fig.7.2: Op amp packages. (a) Metal can, and (b) 8-pin DIP package.



(a) 8-lead metal can (TO-99), top view

(b) 8-lead mini, dip top view

Fig.7.3: Pin diagrams for (a) metal can, and (b) 8-pin dip package of op amp. NC means no connection.

The pin count of every IC including op amps is done as follows. Look at the top view of the IC and note the position of a notch or a dot in case of DIPs and a tab in case of a metal can package. The notch or dot or tab identifies the pin 1 which is on its left. Then other pins are counted counterclockwise. Here is caution. Never count looking at the bottom view.

SAQ 2

What is the way in which the IC pins are counted?

7.2.3 Number Code

On the package of the IC including op amps some numbers are printed with the help of which the IC is identified. On op amp package, say in a typical IC, CA741CP is printed. The first two letters 'CA' identify the manufacture's code. CA is the code for RCA, AD is for Analog Devices, LM is for National Semiconductor Corp, μA is for Fairchild, etc. The word 741C is the circuit designator for commercial purpose op amp. This word for any other IC could be of three to seven numbers and letters. In 741C, C identifies the commercial temperature range (0 to 70°C). Other temperature codes are I for industrial purpose (–25 to 85°C) and M for military purposes (–55 to 125°C). Last letter P stands for plastic package.

SAQ 3

Identify the IC with number code LM741I.

7.2.4 Power Supply

For supplying bias to a general purpose op amp (741C), a bipolar power supply is required. Commercially available dual power supplies which give voltages (+15)–0–(–15)V or (+9) –0– (–9)V are used with the op amps. Such voltage ranges are quite often mentioned as ±15 V or ±9 V. Two equal voltage sources as shown in the Fig.7.4 can also be used with a common terminal.

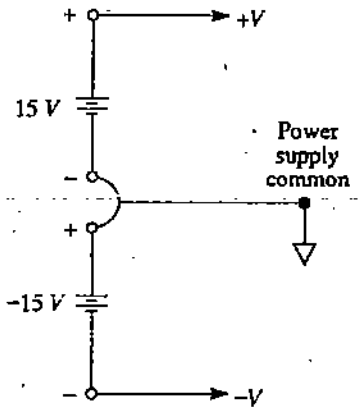


Fig.7.4: Dual power supply.

SAQ 4

Name the pins of op amp 741C to which power supply is connected.

7.2.5 Precautions

A circuit in which op amp is being used is made either on a breadboard or on a printed circuit board. There are certain precautions in making and using the circuit which must always be borne in mind.

— Do the entire wiring of the circuit with power supply off.

— Use Wires as short as possible.

— All ground connections should meet at a common point.

— First of all, power (±V) should be supplied to the op amp.

— Apply signal only after op amp is supplied power.

— Always measure voltages and not currents. The current may be found by finding voltage at two ends of a resistor.

— When the work is over, remove signal first and then switch off op amp power supply.

It is necessary here to stress further that never, never

— reverse the bias polarity,

— apply signal voltages greater then +V and less than −V,

— connect ac signal with op amp power off.

SAQ 5

Can you connect positive terminal of the dual power supply to pin 4 of op Amp 741C and negative terminal to pin 7? Why?

7.3 CHARACTERISTICS OF OP AMPS

The ideal characteristics of an operational amplifier will be outlined in detail later. For the time being, it should be remembered that an ideal operational amplifier has infinite voltage gain, infinite input impedance and zero output impedance.

Actual characteristics of an op amp are as a matter of fact different.

7.3.1 Input-Output Relationship

As pointed out earlier, op amp amplifies the difference of voltage present between the input pins 3 and 2. If the difference voltage is V_D and the gain of the op amp is A, then the output voltage is AV_D. In Fig.7.5, the voltage at pin 3 is designated to be V_1 and at pin 2 it is V_2 Thus

$$V_D = V_1 - V_2$$

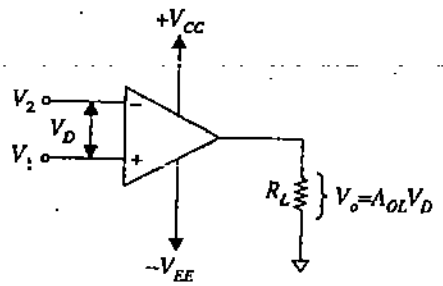


Fig.7.5: Output voltage depends on the input difference voltage.

and the output voltage is

$$V_O = A(V_1 - V_2) = AV_D$$

This gives the voltage gain

$$A = \frac{V_O}{V_D}$$

The voltage gain A in this equation is referred to by several names—large signal voltage gain (LSVG), open loop gain (A_{OL}) or Differential voltage gain (A_D).

Remember that the difference voltage, V_D, has been calculated as follows:

V_D = voltage at pin 3 (V_1) – Voltage at pin 2 (V_2)

Both V_1 and V_2 are measured with respect to the ground. Note that the gain of the ideal operational amplifier is infinite, while for the realistic, say μA741C, the gain is 200,000. Thus theoretically, the output voltage should be 200,000 times V_D. But one cannot obtain from any amplifier a voltage which is greater than the bias voltage supplied by the power supply. Therefore, the output voltage gets stuck to the bias voltage. Actually, the op amps consist of several transistors across which certain voltages are dropped so as to maintain their proper functioning. This limits the output voltage below the bias voltage. The upper limit of the output voltage V_O is the positive saturation voltage, $+V_{SAT}$ and the lower limit is the negative saturation voltage, $-V_{SAT}$. In the case of the general purpose op amp biased with ±15 power supply the $+V_{SAT}$ and $-V_{SAT}$ are +14 V and –13 V respectively restricting the peak-to-peak symmetrical swing to 13 V. It should now be remembered that if the input to pin 3 is greater than that to pin 2, then V_D is positive and the output is above ground and is $+V_{SAT}$. And if the input to pin 2 is greater than that to pin 3, then V_D is negative and the output is below ground and is $-V_{SAT}$.

SAQ 6

How do you calculate input difference voltage to an op amp?

7.3.2 Input Offset Voltage

Input offset voltage is the voltage which is applied between pins 2 and 3 so as to get zero output at pin 6. If the dc input voltages applied to pins 3 and 2 are V_1 and V_2 as shown in Fig.7.6, then the input offset voltage is $V_{10} = V_1 - V_2$ with zero output voltage. The value of V_{10} can be positive or negative. The smaller is the value of V_{10}, better is the matching of input terminals. For 741C, the maximum value of V_{10} is 6 mV.

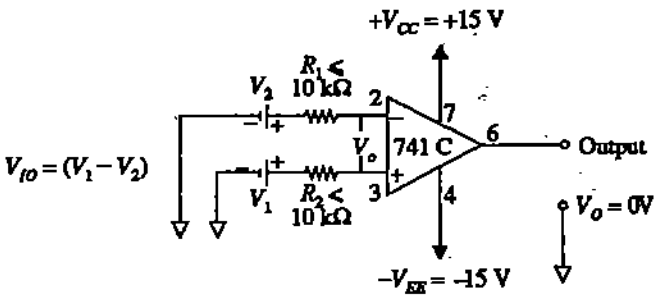


Fig.7.6: Measuring input offset voltage.

7.3.3 Output Offset Voltage

Output voltage of an op amp should be ideally zero when both the inputs are zero or grounded. However, it may not be so. Some output voltage may be available with both the inputs grounded. This voltage is known as output offset voltage and it should be made zero, otherwise the results will be inaccurate.

To reduce the output offset voltage to zero, a carbon potentiometer of high resistance, say 22 kΩ, is connected between the pins 1 and 5, and the wiper is connected to pin 4 as shown in Fig.7.7. Adjust the position of the wiper so that output offset voltage is reduced to zero. In case the output offset voltage is not reduced to zero despite the

adjustments, then a voltage compensating network is designed (which is beyond the course of this unit).

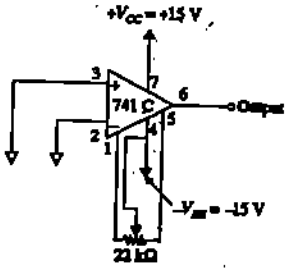


Fig.7.7: Adjusting output offset voltage.

SAQ 7

What is the output offset voltage?

7.3.4 Differential Input Resistance

Differential input resistance, R_I is generally referred to as the input resistance of the op amp. This is the equivalent resistance which can be measured at either of the inputs-inverting or non-inverting with the other terminal grounded. Ideally this resistance is infinite. But in case of 741C, R_I is 2 MΩ.

7.3.5 Output Resistance

Output resistance, R_O is the equivalent resistance measured between the output pin 6 and the ground. Ideally the value of R_O is zero, but for 741C it is 75Ω.

7.3.6 Common Mode Rejection Ratio

There may be situations when the op amp is being used in a noise environment. The pins 2 and 3 may pick up same noise voltages. Since the op amp amplifies the difference in voltage at the two inputs, therefore with the same voltage present at the two inputs the output voltage due to noise should be ideally zero thus cancelling unwanted noise singles. To assess whether both the inputs are properly matched for this purpose a term known as common mode rejection ratio (CMRR) is used. It is defined by several manufacturers in several ways which are essentially equivalent. It is defined as the ratio of the open loop voltage gain, A_{OL}, to the common mode voltage gain, A_{CM}.

$$\text{CMRR} = \frac{A_{OL}}{A_{CM}}$$

The common mode voltage gain, A_{CM}, is obtained as shown in Fig.7.8. Both the inputs are connected to each other and given the same common mode voltage, V_{CM} and the common mode output voltage V_{OCM} is noted. Then the common mode voltage gain is

$$A_{CM} = \frac{V_{OCM}}{V_{CM}}$$

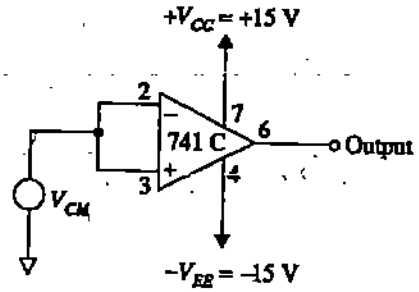


Fig.7.8: Common mode connections.

The A_{CM} should be as small as possible and ideally it should be zero. The CMRR should be very high, ideally infinite. The higher is the CMRR, better is the matching of input terminals and smaller is the V_{OCM}. The CMRR, being large, is measured in decibels (dB). For op amp 741C, it is 90 dB.

SAQ 8

Will you use an op amp with a low CMRR?

7.3.7 Maximum Output Current

Maximum output current obviously flows when the output terminal is shorted out which will damage the op amp. No one likes it to happen even accidentally. All op amps of 741 family have built-in protection circuitry and are protected upto 25 mA of current. Therefore, the maximum output short circuit current is 25 mA.

7.3.8 Power Consumption

The amount of power that is consumed by an op amp to operate properly (with zero input voltage) is defined as the power consumption of the op amp. For 741C, it is 85 mW. The op amp also draws a current of 2.8 mA from the power supply.

7.3.9 Slew Rate

Slew rate indicates how rapidly the output of an op amp changes with the change in the input frequency. It is defined as the maximum rate of change of output voltage (in volts) per unit time (in micro seconds). Thus

$$\text{SR} = \left.\frac{dV_O}{dt}\right|_{\max} \quad \text{V/}\mu\text{s}$$

Slew rate changes with the voltage gain and is normally specified by the manufacturer at the unity closed loop gain (+1). Ideally the slew rate should be infinite. The drawback of 741C is that its slew rate is 0.5 V/μs which limits its use at higher frequencies. For use at higher frequencies other special purpose op amp have to be chosen. The latest op amps – LF351, μAF771, and MC 34001 have slew rate of 13 V/μs, while high speed op amp LM318 has a slew rate of 70 V/μs.

7.3.10 Gain Bandwidth Product

Ideally the operational amplifier has infinite bandwidth, but as the closed loop gain is increased the bandwidth decreases.

Normally it is defined as bandwidth of the op amp when its closed loop gain is 1. For 741C, the gain bandwidth product (GB) is approximately 1 MHz.

7.3.11 Characteristics of Ideal op Amp and 741C

	Ideal	741C
1.	Infinite voltage gain (LSVG, A_{OL}, A_D).	200,000
2.	Infinite input resistance (R_i) (any signal source may be used to give input to the op amp without being loaded by it).	2 MΩ
3.	Zero output resistance (R_O) (output can drive any number of other devices).	75 Ω
4.	Zero output voltage when input is zero.	May not be so. Use high R carbon pot. between pins 1 and 5, connect wiper to pin 4. Adjust wipe. for V_O. = 0.

5.	Infinite CMRR (Common mode noise voltage output is zero).	90 dB
6.	Infinite slew rate (output voltage changes occur simultaneously with input voltage changes).	0.5 V/μs
7.	Infinite bandwidth (BW) (any frequency can be amplified without attenuation).	BW decreases with gain. Refer to GB product ≈ 1 MHz.

7.4 EQUIVALENT CIRCUIT OF AN OP AMP

The equivalent circuit of an op amp is shown in Fig.7.9. In the circuit R_I and R_O input and output resistance of the op amp and AV_D is the equivalent Thevenin voltage source. The value of A, R_I and R_O are available from the manufacturer's data sheet.

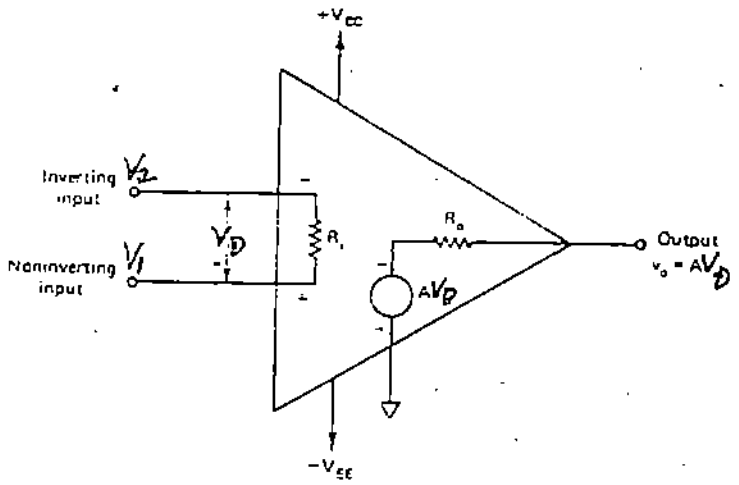


Fig.7.9: Equivalent circuit of an op amp.

7.5 IDEAL VOLTAGE TRANSFER CURVE

Fig.7.10 shows a plot drawn not to the scale, between the difference input voltage, V_D, and the output voltage, V_O. The curve in the plot is known as ideal voltage transfer curve. If V_D is positive, V_O reaches $+V_{SAT}$ and if it is negative than $-V_{SAT}$. Thus output voltage cannot be greater than $+V_{SAT}$ and less than $-V_{SAT}$. If the plot is drawn to the scale, then curve will be vertical straight line.

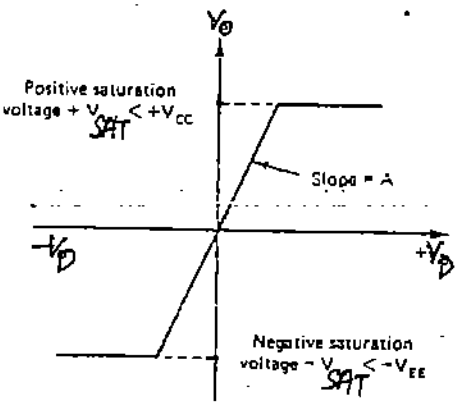


Fig.7.10: Ideal voltage transfer curve.

7.6 COMPARATORS

7,6,1 Voltage Level Detector

Recall that an operational amplifier is a difference amplifier and that its maximum output voltage is $\pm V_{SAT}$. Fig.7.11 shows a circuit for an op amp used as a comparator. A fixed reference voltage V_{REF}, say of 1V, is applied to inverting input pin 2. The time dependent signal V_{in} is applied to the non-inverting input pin 3. The output voltage V_O is

$$V_O = AV_D$$
$$= A\,(V_{in} - 1\text{V}).$$

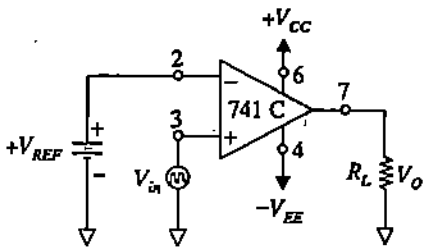


Fig.7.11: Comparator or voltage level detector.

Now, if $V_{in} = 1V_D$, then $V_D = 0$. Hence $V_O = 0$ as shown in Fig.7.12 and 7.13. If $V_{in} > 1$ V, then V_D is positive. In this case the output gets limited to $+V_{SAT}$ as shown in Fig 7.12. If $V_{in} < 1$V, then V_D is negative which limits the output to $-V_{SAT}$. Thus at any instant of time the output voltage V_O shows whether the input is greater than V_{in} or less than V_{in}. This circuit acts like an analog to digital converter. This non-inverting comparator is also known as voltage level detector. The value of V_{REF} can be 0, or any value positive or negative. It can also be connected to any of the inputs. However, to find the output waveform, one must note whether V_D is positive or negative. If the reference voltage V_{REF} is connected to the non-inverting input pin 3 and the input signal is given to pin 2, the comparator is known as inverting comparator.

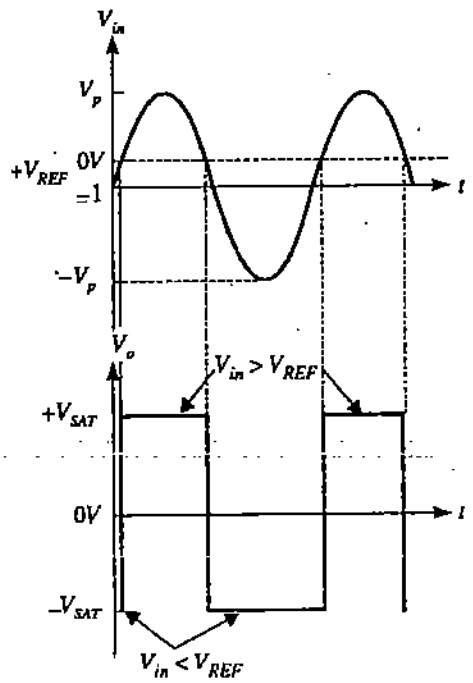


Fig.7.12: Output waveform of the comparator with $+V_{REF}$

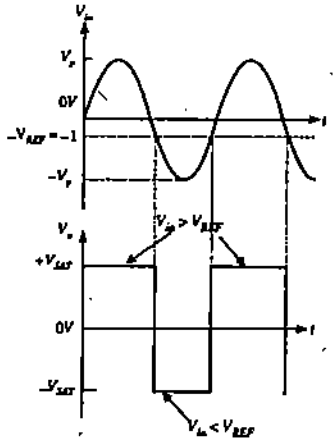


Fig.7.13: Output waveform of the comparator with $-V_{REF}$

7.6.2 Zero Crossing Detector

The zero crossing detector is an application of comparators. Fig.7.14 shows a circuit for zero crossing detector in which pin 3 is grounded making the ground potential (0V) to be the reference voltage. The input signal is given to pin 2. When the V_{in} exceeds 0V, then V_D is negative and the V_O is limited to $-V_{SAT}$. Likewise, when V_{in} is less than 0V, then V_D is positive and the V_O is limited to $+V_{SAT}$. Thus the output voltage shows whether the input voltage is above or below the zero level as is shown in Fig.7.15.

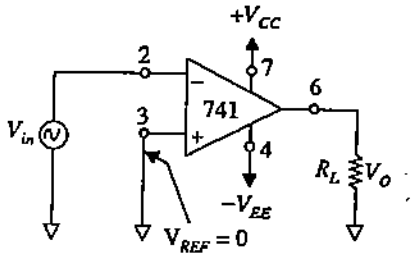


Fig.7.14: Zero crossing detector.

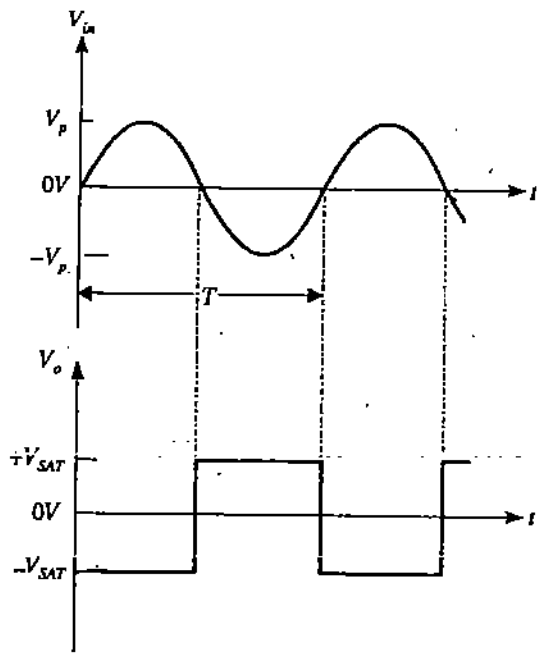


Fig.7.15: Input and output waveforms of a zero crossing detector.

SAQ 9

Trace the output voltage waveform of the circuit given in Fig.7.16.

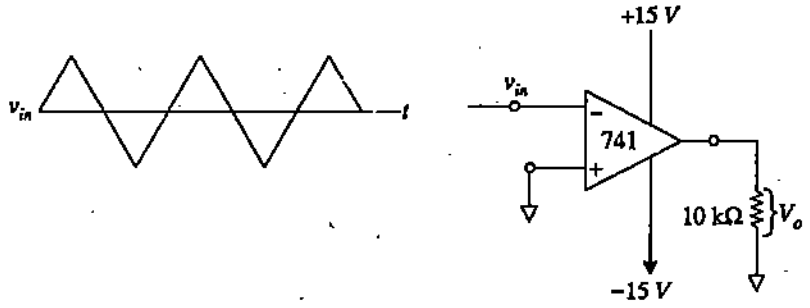


Fig.7.16

7.7 SUMMARY

- Several manufacturers use a combination of op amp symbol and IC package to give the pin-out diagram.
- The name of the manufacturer the op and amp temperature range can be found out by reading the number code printed on the top of the IC package.
- A dual power supply is needed to operate the op amp.
- Input signal should be given to the op amp only after supplying bias voltage to it.
- Polarity of the bias supply voltages to pin 4 and 7 should never be reversed.
- The ideal operational amplifier has infinite voltage gain, input resistance, CMRR and slew rate.
- The ideal operational amplifier also has zero output resistance and output offset voltage.
- The realistic characteristics are markedly different than the ideal characteristics. However, in comparative terms they can be taken to be ideal.
- The equivalent circuit of an ideal op amp is quite often used in the analysis of the basic operating principles of op amps.
- The voltage transfer curve of an op amp is the curve between the output voltage and the difference input voltage.
- Comparators are basically voltage level detectors with reference voltage source connected to either of the inputs of the op amp. Reference voltage can be 0, positive or negative.
- Inverting and non-inverting comparators and zero crossing detectors are used in many applications.

7.8 TERMINAL QUESTIONS

1) Give the pin-out diagram of op amp DIP 741C.
2) What are the precautions that must always be kept in mind while working with op amps?
3) Distinguish between characteristics of an ideal op amp and that of 741C.
4) Trace the output waveform of the circuit given in Fig.7.17.

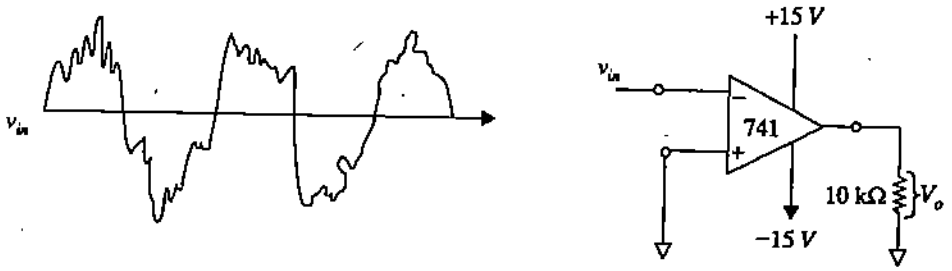


Fig.7.17

5) If the input pin 2 is grounded and a triangular wave input is given to pin 3, then what will be the output waveform?

7.10 SOLUTIONS AND ANSWERS

SAQs

1. Inverting input pin 2, non-inverting input pin 3 and the output pin 6.
2. See the top view of the IC. Look for the notch or dot on the body of the IC. The pin on the left of the notch or dot is pin 1. Then start counting pins counter-clockwise.
3. For the IC with number LM741I, the letters LM identify the name of the manufacturer, National Semiconductor Corp. The letters 741 indicate op amp. The letter I indicates the temperature range for the industrial purposes, i.e. –25° to 85°C. Thus LM741I means that it is an op amp manufactured by National Semiconductor Corp, for industrial purpose for a temperature range of –25° to 85°C.
4. Pins 4 and 7. $-V_{EE}$ is connected to pin 4 and $+V_{CC}$ is connected to pin 7.
5. No. It will permanently damage the op amp.
6. Input difference voltage to an op amp V_D is calculated as follows:

   V_D = voltage at pin 3 (V_1) – voltage at pin 2 (V_2)
7. It is the voltage available at the output pin 6 even when both the input pins 2 and 3 are grounded.
8. No. Higher is the CMRR, better is the matching of input terminals.
9. The output waveform is as shown in Fig.7.18.

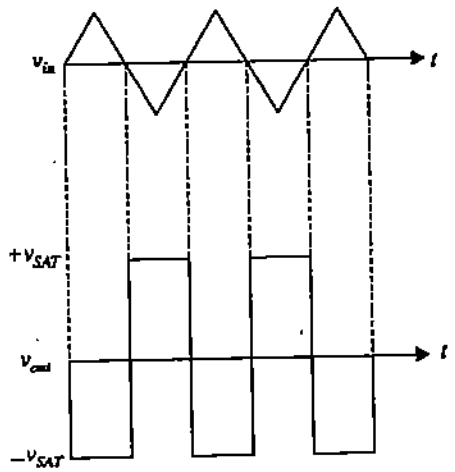


Fig.7.18

TQs

1) Given in Fig.7.3 (b).
2) Listed in section 7.2.5.
3) Given in section 7.3.11.
4) Output waveform is given in Fig.7.19.

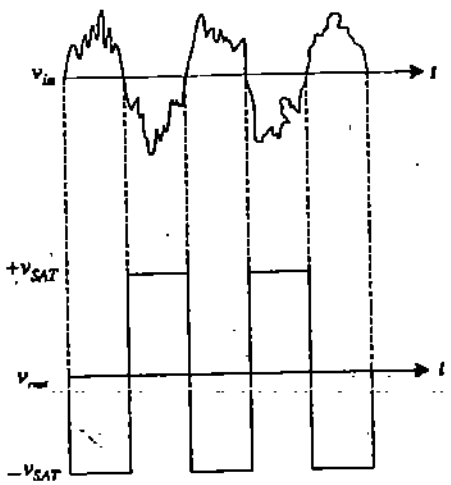


Fig.7.19

5) The circuit for this question and the output waveform are as shown in Fig.7.20.

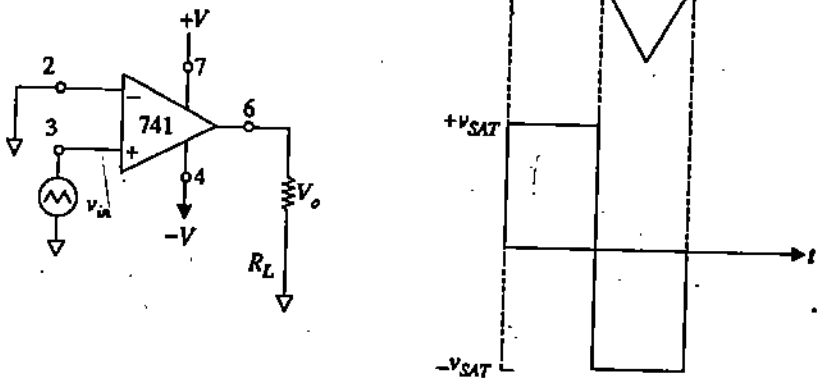


Fig.7.20

UNIT 8 APPLICATIONS OF OPERATIONAL AMPLIFIERS

Structure

8.1 INTRODUCTION

The infinite open loop gain, A_{OL} of an ideal op amp or as high A_{OL} as 200,000 for realistic op amp 741C is of no use for most applications in which op amp can be used. The open loop gain is also not a constant. It varies with changes in the temperature, power supplied, and manufacturing techniques. With such a large gain, the output corresponding to a small input voltage gets clipped to $+V_{SAT}$ or $-V_{SAT}$. Moreover for output voltages within the saturation voltages, the input voltages, have to be of the order of a few microvolts. Such low voltages are difficult to obtain even in laboratories. Since in linear amplifiers the output voltage is proportional to the input voltage, therefore the open loop operational amplifiers cannot be used. However, in certain applications like comparators (already discussed in Unit 9) and square wave generators open loop amplifiers are used.

In order for using the op amp in linear amplifiers and most other applications, it is essential to design some external circuit. Such a circuit is made using the concept of negative feedback which will be discussed later in section 8.7. In this application based Unit, unless stated otherwise, we shall use op amp 741C. The output pin is connected to the inverting input pin 2 using a resistor. It can be shown that the gain of such an amplifier with negative feedback, which is known as the closed loop gain, A_{OL} is totally independent of the open loop gain, A_{OL} of the op amp and depends only upon external circuit parameters.

Objectives

After studying this unit, you should be able to:

- draw the circuit diagram for the inverting amplifier and find out its closed loop gain, A_{CL},
- use an inverting amplifier as a multiplier or divider,
- design an inverting amplifier with a particular gain,
- draw a circuit diagram for a non-inverting amplifier and find out its closed loop gain,
- draw a circuit diagram for an inverting adder and use this circuit for a channel amplifier,

- draw the circuit diagram for a basic differentiator and show that the output of such a circuit is the derivative of the input waveform,
- draw the circuit diagram for a basic integrator and show that the output of such a circuit is the integral of the input waveform,
- explain the concept of feedback in amplifiers.

8.2 INVERTING AMPLIFIER

Introduction

Consider the circuit given in the Fig.8.1. In this circuit the output pin 6 is connected through a resistor R_F to the inverting input pin 2. The input voltage is given to pin 2 through an input resistor R_I. The inverting input pin 3 is grounded. The output pin 6 is also grounded through a resistor R_L. In this circuit, two realistic but very simplifying assumptions are made which are as follows. If the output voltages is not in saturation then the differential input is zero and the current entering into inverting and non-inverting input pins is negligible.

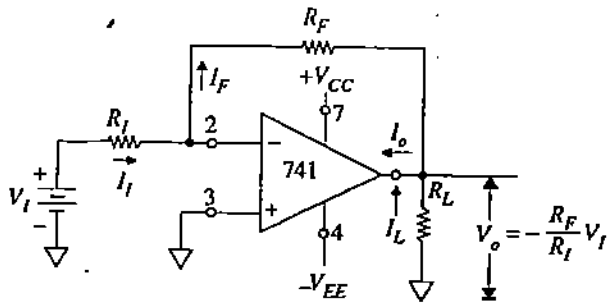


Fig.8.1: Inverting amplifier.

Positive input

A positive input voltage ($+V_I$) is applied to the inverting (–) input pin 2 through input resistor R_I and the feedback resistor R_F provides the necessary feedback from the output to the input. As per the realistic assumptions made above, no current is entering into the op amp through pin 2. And because non-inverting (+) input pin 3 is grounded, therefore pin 2 is also at ground voltage, i.e. 0V. Thus though the pin 2 is not connected to the ground, yet it virtually appears to be grounded. It should be noted that in the equivalent circuit of an op amp (Fig.7.9) pins 2 and 3 are connected to each other through a very high resistance (ideally infinite). We, therefore, say that pin 2 or the inverting input is at virtual ground.

In the circuit of Fig.8.1, the current through R_I is decided by the voltage drop across it. One end of R_I is connected to $+V_I$ and another end is at 0V. Therefore, the voltage drop across R_I is $+V_I$. The input current, I_I, flowing through R_I from a point of higher potential to a point of lower potential (i.e. pin 2 which is at 0V) is

$$I_I = \frac{V_I}{R_I} \tag{8.1}$$

Since the current does not enter the op amp, therefore I_I has to flow through R_F. Therefore, I_F, the current flowing through R_F is equal to I_I. That is $I = I_I = I_F$. Thus the voltage drop across R_F is

$$V_F = IR_F \tag{8.2}$$

Putting for I from Eq. (8.1) we get

$$V_F = \frac{V_I}{R_I} R_F \qquad (8.3)$$

Since pin 2 is at virtual ground, R_L is in parallel with R_F. Therefore, the magnitude of V_F is equal to V_O. But V_F is negative because the current flows from pin 2 (which is at 0V) to pin 6. Thus, V_O the voltage between pin 6 and ground is

$$V_O = - V_F$$

$$= - \frac{V_I}{R_I} R_F = - \frac{R_F}{R_I} V_I \quad \text{(using Eq. 8.3)}$$

The closed loop gain of the amplifier, A_{CL}, is

$$A_{CL} = \frac{V_O}{V_I} = - \frac{R_F}{R_I} \qquad (8.4)$$

Thus A_{CL} depends on R_F and R_I only and does not at all depends on the open loop gain operational amplifier. Since A_{CL} is negative, that is may we call this configuration of the amplifier as inverting amplifier. The choice of R_F and R_I is in the hands of the designer and the gain of practically any value can be obtained. In all practical applications the value of R_I should be chosen to be large, say 10 kΩ, so that it does not short out the input resistance of the op amp.

The output current I_O is the sum of the current I flowing through R_I and the current $I_L = V_O/R_L$ flowing through the load R_L. Thus

$$I_O = I + I_L \qquad (8.5)$$

While designing an op amp based amplifier, the amount of current required at the output should also be kept in mind. The value of I is set by V_I and R_I which are in turn set by the design requirement. Thus, the output current I_O is controlled by proper choice of R_L.

The inverting amplifier circuit can be used for multiplication and division. The output voltage is R_F/R_I times the input voltage. If the input voltage represents some number then the output voltage will be equal to that number multiplied by the factor R_F/R_I. The ratio R_F/R_I is under the control of the user and can assume any value. By making R_I greater than R_F, the inverting amplifier can be used for division.

Example:

Design an amplifier using op amp 741C and V_I of 1V for a gain of –8 and with I_O of 0.9 mA.

Solution:

Choose R_I = 10 kΩ.

with A_{CL} = –8, $R_F = -8R_I$ = 80 kΩ.

Using equation (8.1)

$$I = \frac{V_I}{R_I} = \frac{1\text{V}}{10\ \text{k}\Omega} = 0.1\ \text{mA}$$

From equation (8.5),

$$I_L = I_O - I = 0.9\,\text{mA} - 0.1\,\text{mA} = 0.8\,\text{mA}$$

$$V_O = 1V_O \times (-8) = -8\text{V}$$

$$I_L = \frac{V_O}{R_L}$$

Or $$R_L = \frac{V_O}{V_D} = \frac{8\text{V}}{0.8\ \text{mA}}\ 10\,\text{k}\Omega.$$

Hence, for the required design R_I = 10 kΩ and R_F = 80 kΩ and R_L = 10 kΩ. The dc bias for the op amp should be well above the expected output. In this example V_O is −8V, therefore a ±9V power supply will not be a good choice, for −8V would be just equal to $-V_{SAT}$. Therefore, a greater value of power supply is chosen, ±10V or above.

SAQ 1

What is the output voltage in the circuit given below?

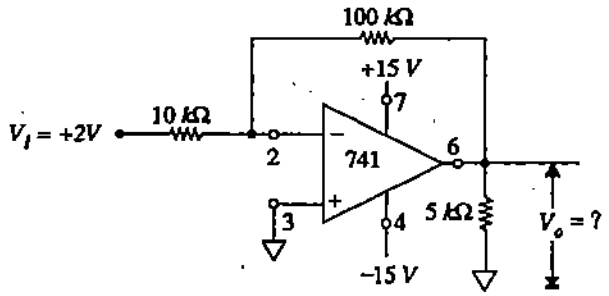


Fig.

8.3 NON-INVERTING AMPLIFIER

The circuit given in Fig.8.2 is for a non-inverting amplifier. In this circuit R_I continue to be connected as in the case of inverting amplifier except that the R_I is ground as shown and the input voltage V_I is given to the non-inverting (+) input pin 3.

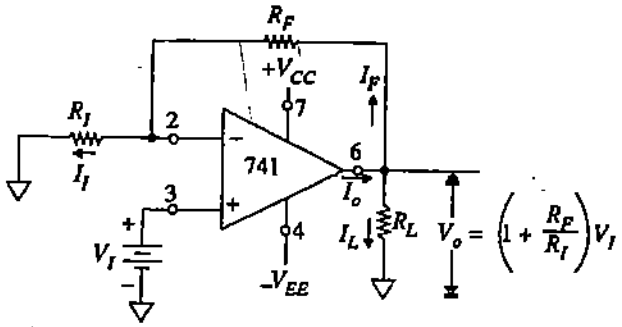


Fig.8.2: Non-inverting amplifier.

For the reasons discussed in the previous section, the inverting input pin 2 is also at the same voltage at which non-inverting input pin 3 is. Thus, the pin 2 is at $+V_I$ which sets the current I_I through R_I. The voltage drop across R_I being V_I, we get

$$I_I = \frac{V_I}{R_I} \tag{8.6}$$

Obviously, I_I flows from pin 2 to the ground. For the same reasons, I_F the current flowing through R_F has to be equal to I_I, i.e. $I = I_1 = I_F$. Thus, the current I flows from output terminal pin 6 to pin 2 to ground. Hence, the output pin 6 is at a greater potential than pin 2. Since the load resistor R_L is now in parallel with the series

combination of R_I and R_F therefore the output voltage is equal to the sum of voltage across R_I and R_F. Thus

$$V_O = V_I + IR_F$$

$$= V_I + \frac{V_I}{R_I} R_F \quad \text{(using Eq. 8.6)}$$

$$= V_I(1 + \frac{R_F}{R_I})$$

Or the closed loop gain of the amplifier is

$$A_{CL} = \frac{V_O}{V_I} = (1 + \frac{R_F}{R_I}) \tag{8.7}$$

Notice that A_{CL} has the same sign as the input voltage V_I i.e. positive. For this reason, we call such an amplifier to be a non-inverting amplifier. Notice further that in this case also the gain depends upon the values of R_F and R_I and not on the parameters of the operational amplifier. However, the gain is always greater than unity. The ratio R_F/R_I can be made as small as possible and the gain can be made close to unity, but it can never be less than unity. Pin 6 being at a potential greater than the ground potential, therefore the load current I_L flows from pin 6 to ground through the load resistor R_L.

Example:

Design an amplifier using op amp 741C and V_I of 0.2V for a gain of +10 with I_O of 0.1 mA.

Solution:

Choose $R_I = 10\,\text{k}\Omega$.

Given $A_{CL} = +10 = 1 + (R_F/R_I)$

or $R_F/R_I = 10 - 1 = 9$

or $R_F = 9R_I = 90\,\text{k}\Omega$

$I = V_I/R_I = 0.2\text{V}/10\ \text{k}\Omega = 0.02\,\text{mA}.$

$V_O = +10V_I = 10 \times 0.2\text{V} = 2\text{V}$

From $I_O = I + I_L$, we get

or $I_O = 0.02 + V_O/R_L = 0.1\,\text{mA}$

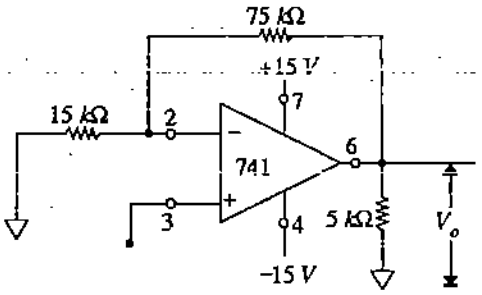
or $V_O/R_L = (0.1 - 0.02)\text{mA} = 0.08\,\text{mA}$

or $R_L = 2\text{V}/0.08\,\text{mA} = 25\,\text{k}\Omega.$

Hence, for the required design $R_I = 10\,\text{k}\Omega$, $R_F = 90\,\text{k}\Omega$ and $R_I = 25\,\text{k}\Omega$.

SAQ 2

What is the gain of the amplifier shown in the figure given below?



8.4 INVERTING ADDER

The inverting amplifier configuration of the op amp is useful in many applications. The inverting amplifier can be used for multiplication and division as stated in section 8.2. The circuit of Fig.8.1 has only one input through R_I. The number of inputs can be increased to any number. Consider the circuit given in Fig.8.3 in which there are three resistors as input resistors connected to pin 2 and a common R_F for all the R_I's. Since the pin 3 is grounded, pin 2 is at 0V.

The current flowing through R_F is the sum of all the currents reaching summing point S at pin 2. These current are set by V_{I1} and R_{I1} V_{I2} and R_{I2} and V_{I3} and R_{I3}. Therefore,

$$I_F = I_{I1} + I_{I2} + I_{I3}$$

$$= \frac{V_{I1}}{R_{I1}} + \frac{V_{I2}}{R_{I2}} + \frac{V_{I3}}{R_{I3}}$$

The output voltage V_O is

$$V_O = - I_F \cdot R_F$$

$$= -\left(\frac{V_{I1}}{R_{I1}} + \frac{V_{I2}}{R_{I2}} + \frac{V_{I3}}{R_{I3}}\right) R_F \qquad (8.8)$$

And if all the resistors are of same value, i.e $R = R_F = R_{I1} = R_{I2} = R_{I3}$ then we get

$$V_O = - (V_{I1} + V_{I2} + V_{I3}) \qquad (8.9)$$

Thus the output of this circuit is the sum of all the input voltages. This circuit is known as inverting adder. The negative sign indicates 180° phase change between the input and the output.

If all the R_I's are chosen to be same and R_F is of different value then the output voltage will be

$$V_O = - (V_{I1} + V_{I2} + V_{I3}) \qquad (8.10)$$

This equation indicates that the sum of the input is multiplied by a factor R_F/R_I which is under the control of the user. In this equation if R_F/R_I is made equal to 1/3, then the resulting amplifier is averaging amplifier.

The circuit of Fig.8.3 has several applications. Apart from the applications mentioned above if the circuit is made with different values of R_I's as shown, then Eq.8.8 suggests that the output voltage is the sum of all the outputs corresponding to each input. Such a circuit is also used in digital to analog conversion (which will be discussed in Unit 12, Block 4). Alternatively, all the inputs need not be used. Only one may be used at a time. In that situation, this circuit is being used for different gains set by different R_I's. Such a circuit can be used as a channel amplifier.

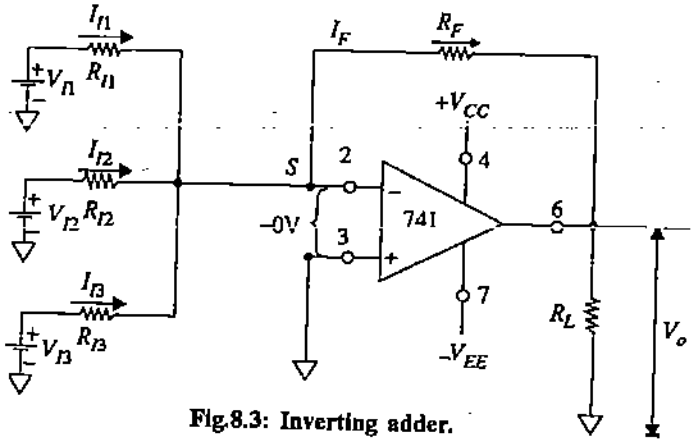


Fig.8.3: Inverting adder.

Example:

Design a 4-channel inverting amplifier using op amp 741C with gains –20, –15, –10, and –5.

Solution:

Make a 4-input inverting amplifier circuit as shown in Fig.8.4. The Eq.8.8 is rewritten for four inputs as follows

$$V_O = -\left(\frac{V_{I1}}{R_{I1}} + \frac{V_{I2}}{R_{I2}} + \frac{V_{I3}}{R_{I3}} + \frac{V_{I4}}{R_{I4}}\right) R_F$$

$$= -\left(V_{I1}\frac{R_F}{R_{I1}} + V_{I2}\ \frac{R_F}{R_{I2}} + V_{I3}\ \ \frac{R_F}{R_{I3}} + V_{I4}\ \frac{R_F}{R_{I4}}\right) \qquad (8.11)$$

It is clear that the gain of each channel can be changed independently by changing the input resistor. We have

$$A_{CL1} = \frac{R_F}{R_{I1}}, A_{CL2} = \frac{R_F}{R_{I2}}, A_{CL3} = \frac{R_F}{R_{I3}}, A_{CL4} = \frac{R_F}{R_{I4}}$$

Choose the value of R_I equal to 10 kΩ for the channel with the highest gain, i.e –20 in this example. Find out the value of R_F as

$$A_{CL1} = -20 = \frac{R_F}{R_{I1}} = \frac{R_F}{10\ \text{k}\Omega}$$

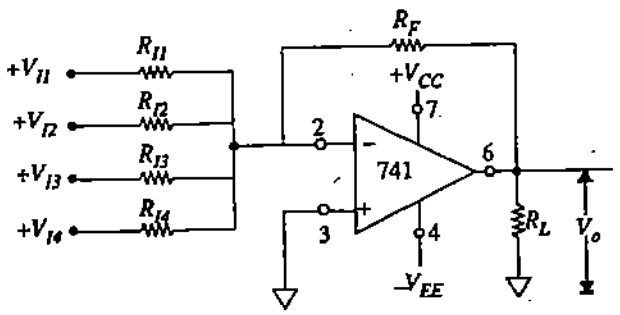


Fig.8.4: Four-input inverting amplifier.

Thus $R_F = 20 \times 10 = 200\,\text{k}\Omega$. With the thus obtained value of R_F find the values of R_I's for other channels.

For channel 2, $A_{CL2} = -15 = 200/R_{I2}$

or $R_{I2} = 200/15 = 13.33\,\text{k}\Omega$

For channel 3, $A_{CL3} = -10 = 200/R_{I3}$

or $R_{I3} = 200/10 = 20\,\text{k}\Omega$

For channel 4, $A_{CL4} = -5 = 200/R_{I4}$

or $R_{I4} = 200/5 = 40\,\text{k}\Omega$.

The design result can be summarised as follows

$R_F = 200\,\text{k}\Omega$

Channel	A_{CL}	R_I
1	−20	10 kΩ
2	−15	13.33 kΩ
3	−10	20 kΩ
4	−5	40 kΩ

SAQ 3

What is the output of the circuit given below?

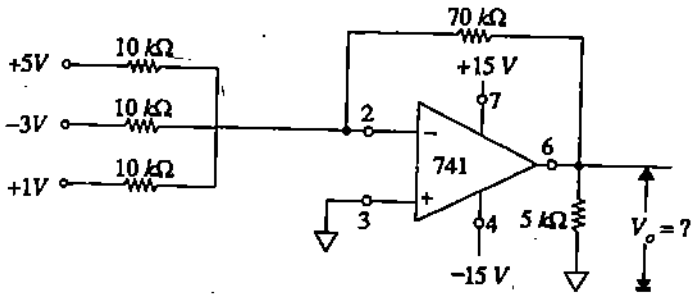


Fig.

8.5 BASIC DIFFERENTIATOR

Fig.(8.5) shows the circuit for basic differentiator which performs the mathematical operation of differentiation. The output waveform is the derivative of the input waveform. The differentiator circuit is obtained by replacing R_I of an inverting amplifier by a capacitor, while rest of the circuit remains the same. For the reasons discussed in the case of inverting amplifier, the current I_C flowing through the capacitor C should be equal to the current I_F flowing through the resistor R_F. Thus

$$I_C = I_F$$

The current I_C flows from the generator to pin 2 from where it flows through R_F. The pin 2 being at 0V, the voltage drop across C is V_I and the drop across R_F is $-V_O$. Recall that the current flowing through a capacitor C is C times the rate of change of voltage across the capacitor. Therefore

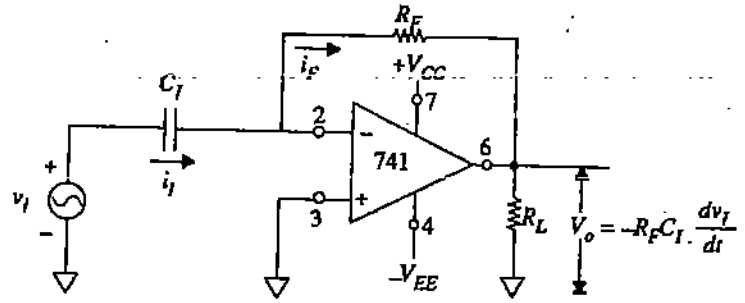


Fig.8.5: Basic differentiator.

$$I_C = C_I \frac{dV_I}{dt}$$

and $$I_F = -\frac{V_O}{R_F}$$

Thus we get

$$C_I \frac{dV_I}{dt} = -\frac{V_O}{R_F}$$

Rearranging, we get

$$V_O = -R_F C_I \frac{dV_I}{dt}$$

If the product $R_F C_I = 1$, then

$$V_O = -\frac{dV_I}{dt} \tag{8.12}$$

Thus the output voltage is the negative derivative of the input voltage V_I. If the input waveform is a sine wave, then the output waveform will be a cosine wave. And if the input waveform is a square wave, then the output waveform will be a spike wave from as shown in the Fig.8.6.

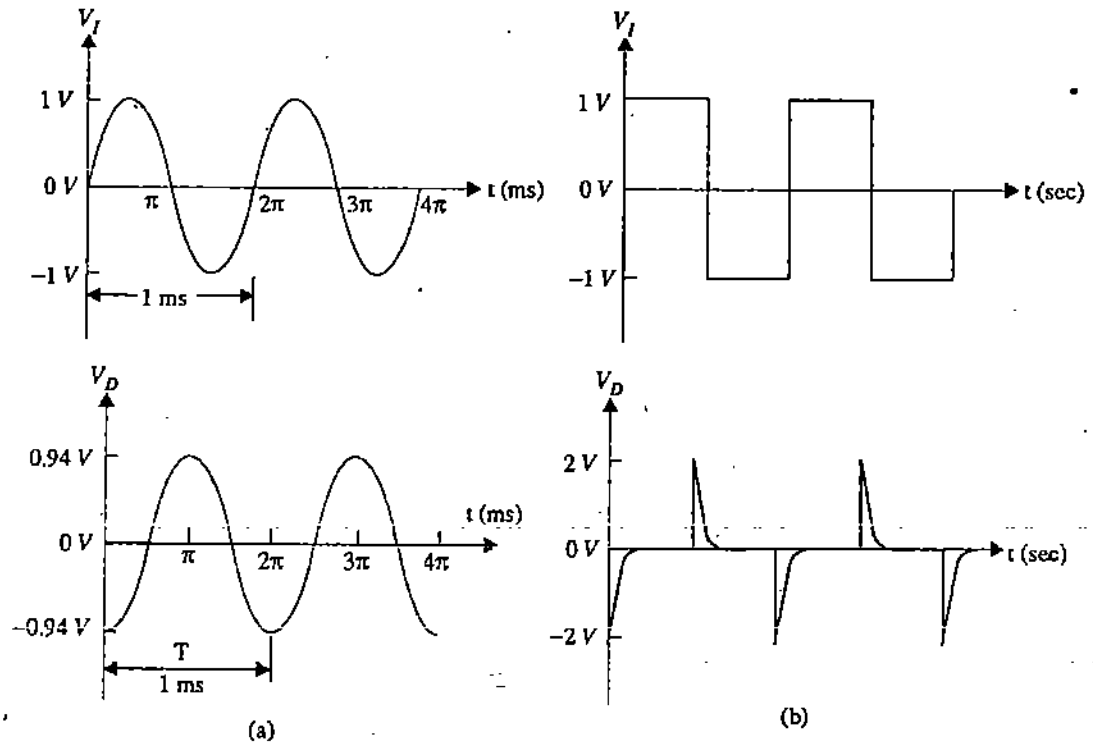
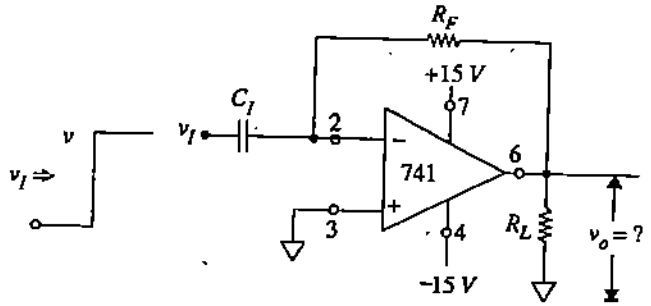


Fig.8.6: Output of a basic differentiator when input is (a) sine wave and (b) square wave.

SAQ 4

Find the output waveform for the basic differentiator shown below.



8.6 BASIC INTEGRATOR

Fig.(8.7) shows the circuit for a basic integrator which performs the mathematical operation of integration. The output waveform, V_O, is the integral of the input waveform, V_I. The integrator circuit is obtained by replacing the resistor R_F by a capacitor C_F in the circuit of inverting amplifier, while rest of the circuit remaining same. For the reasons stated in the case of inverting amplifier, the current I_I flowing through the resistor R_I has to be equal to the current I_F flowing through the capacitor C_F. Thus

$$I_I = I_F$$

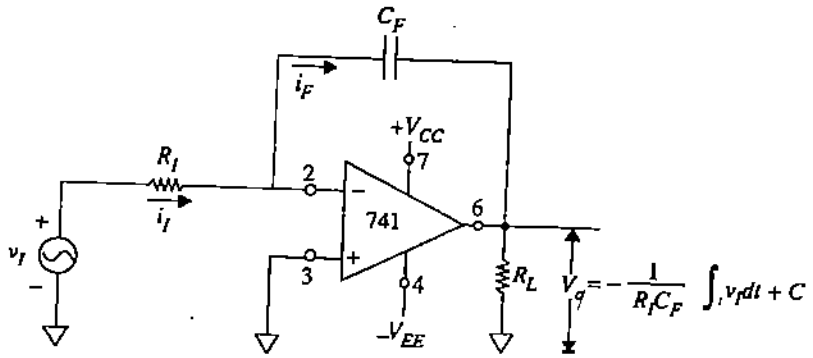


Fig.8.7: Basic Integrator.

The current I_I flows from the generator to pin 2 and from it flows through the capacitor C_F. The pin 2 being at 0V, the voltage drop across $R_I = V_I$ and that across C_F is $-V_O$. Therefore,

$$I_I = \frac{V_I}{R_I}$$

and

$$I_F = C_F \frac{d(-V_O)}{dt}$$

Thus

$$\frac{V_I}{R_I} = C_F \frac{d(-V_O)}{dt}$$

or $$\frac{V_I}{R_I}\,dt = C_F \frac{d}{dt}\,(-V_O)\,dt$$

$$= C_F\,(-V_O) + \text{constant of integration}$$

or $$V_O = -\frac{1}{R_I C_F}\int V_I\,dt + \text{constant of integration} \qquad (8.13)$$

The constant of integration is proportional to the value of V_O at time $t = 0$. The Eq.(8.13) shows that the output is directly proportional to the integral of the input voltage waveform. If the product $R_I C_F$ is made equal to 1 and constant of integration is 0, then we get

$$V_O = -\int V_I dt \qquad (8.14)$$

If the input waveform is sine wave then the output waveform is cosine wave. And if the input waveform is a square wave, then the output waveform is a triangular wave as shown in Fig.8.8.

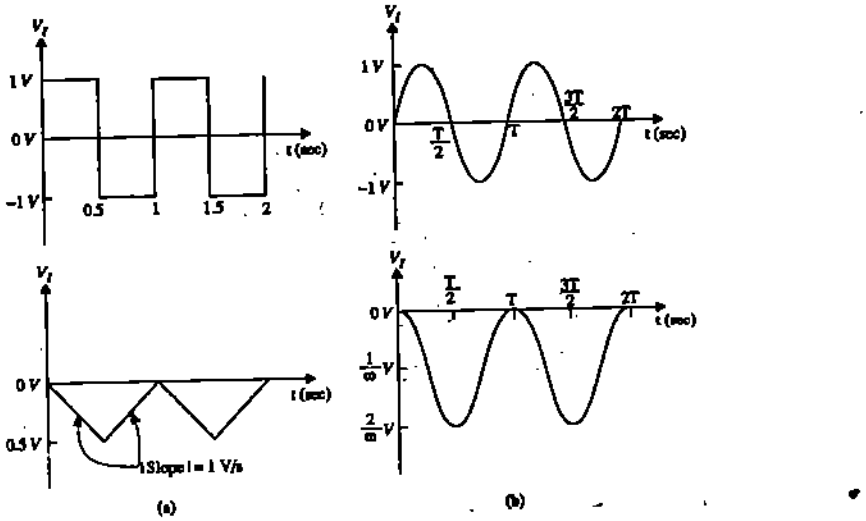
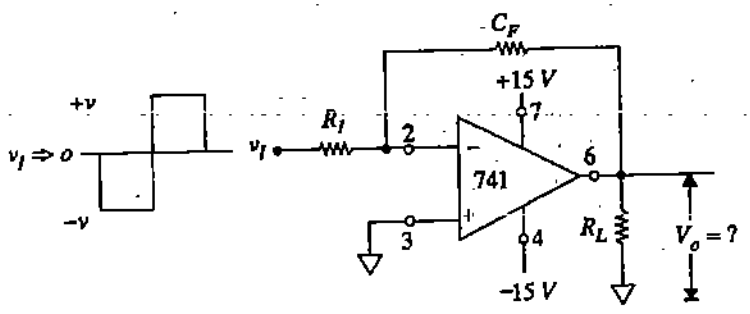


Fig.8.8: Output of a basic integrator when input is (a) square wave. (b) sine wave and

SAQ 5

Trace the output waveform for the basic integrator shown below.



8.7 FEEDBACK IN OP AMP

In the beginning of this unit, two simplifying assumptions were made. Consequently, it was practically taken that no current enters the pin 2 and the current flowing through R_I has to be equal to that flowing through R_F. The pins 2 and 3 were also taken at the same potential. This made the derivations to be quite simplistic. However, the situation is not so. Some current, howsoever small, enters the op amp giving rise to some voltage drop across the input. A mention was made about the negative feedback, but it was not described. Let us see whether the realistic analysis of the circuits used above leads to the same results. The closed loop amplifiers considered above have all been negative feedback amplifiers.

In an amplifier with feedback, there are two basic networks. One is the amplifier and another is feedback network which feeds back a part of the output voltage to the input. If the feedback voltage adds to the input voltage, then the feedback is known as positive feedback. Positive feedback increase the gain. If the feedback voltage is such that it decreases the input voltage, then the feedback is known as the negative feedback. Negative feedback decreases the gain. A description of advantages and disadvantages of negative and positive feedback is beyond the scope of this unit. Therefore, this aspect will not be considered here.

Consider the circuit shown in Fig.8.9. The output terminals are connected to the feedback network and the output of the feedback network is connected in series with the input voltage source. Thus the input voltage V_I in this configuration goes to the non-inverting input pin 3 and the feedback voltage V_F goes to the inverting input pin 2.

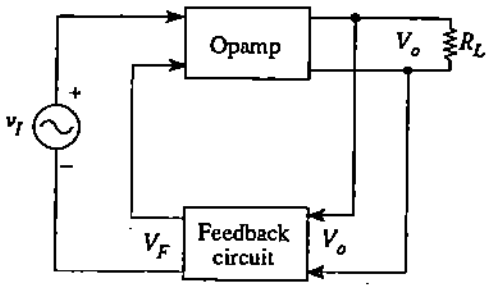


Fig.8.9: Feedback in op amp.

Let us consider the non-inverting circuit of Fig.8.2 which is redrawn here as shown in Fig.8.10. Comparing this circuit with that of Fig.8.9, we find that R_I and R_F form a feedback network. The output voltage V_O is dropped across the series combination of R_I and R_F. The voltage drop across R_I is the feedback voltage V_F and is applied to the inverting input pin 2. The input voltage V_I is applied to the non-inverting input pin 3.

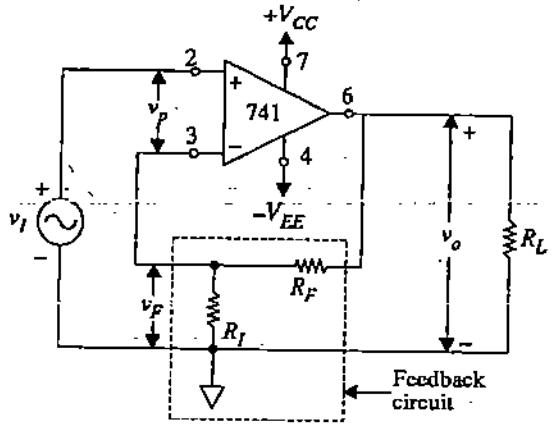


Fig.8.10: Non-inverting amplifier circuit of Fig.8.2 redrawn.

Recall that the closed loop gain A_{CL} is defined as

$$A_{CL} = \frac{V_O}{V_I}$$

The output voltage V_O, in the circuit of Fig.8.10 is

$$V_O = A_{CL}\,(V_1 - V_2) \tag{8.15}$$

where V_I is the input voltage V_I and V_2 is the feedback voltage V_F. Thus considering division of V_O by the feedback network across R_I and R_F, we get

$$V_2 = V_F$$

$$= \frac{R_I V_O}{R_I + R_F} \tag{8.16}$$

Putting for V_1 and V_2 in Eq.(8.15), we get

$$V_O = A_{OL}\,(V_I - \frac{R_I V_O}{R_I + R_F})$$

Rearranging, we get

$$V_O = \frac{A_{OL}\,(R_I + R_F) V_I}{R_I + R_F + A_{OL} R_I}$$

$$A_{CL} = \frac{V_O}{V_I} = \frac{A_{OL}\,(R_I + R_F)}{R_I + R_F + R_I A_{OL}}$$

Since the value of A_{OL} is ideally infinite, and for op amp 741C it is 200,000, i.e. $\sim 10^5$, therefore

$$A_{OL} R_I >> R_I + R_F$$

Thus

$$A_{CL} = \frac{A_{OL}\,(R_I + R_F)}{A_{OL}\,R_I} = \frac{R_I + R_F}{R_I}$$

$$A_{CL} = 1 + \frac{R_F}{R_I}$$

Thus the equation for A_{CL} for the non-inverting amplifier is same as obtained earlier in section 8.3 through the Eq.(8.7). Hence the assumptions made by us in the beginning did not cause any mathematical error, rather helped us solving various networks in a simplified way.

8.8 SUMMARY

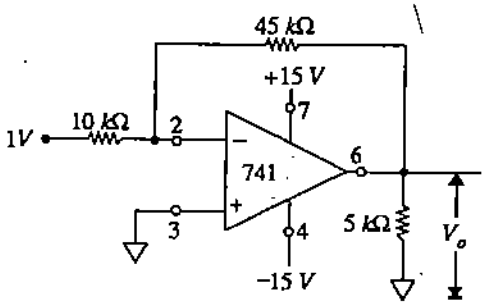
- Infinite open loop gain of an ideal op amp is of no use in most of the applications of the op amp, and therefore external circuitary is used to control the gain of the amplifier.
- With the use of the feedback resistor R_F connecting pins 6 and 2, the closed loop gain of an op amp can be controlled.
- Inverting amplifier gain is absolutely dependent on the feedback resistor R_F and input resistor R_I. Negative sign in the equation for its gain means that there is a phase change of 180° between the input voltage and the output voltage. Because of this reason, it is called inverting amplifier. Input voltage is supplied to pin 2 in this case.

- Inverting amplifier can be used as a multiplier and divider.
- In non-inverting amplifier, there is no phase change between the input and output voltages. The input is given to the pin 3. The closed loop gain of this amplifier is always greater than unity.
- Inverting amplifier can have several inputs with common feedback resistor. Such a circuit can be used as an adder, average and channel amplifier.
- In a basic differentiator, the input resistor is replaced by a capacitor. The output waveform of the differentiator is the derivative of the input waveform.
- In a basic integrator, the feedback resistor is replaced by a capacitor. The output waveform of the integrator is the integral of the input waveform.
- Closed loop gain of the op amp can also be derived from the negative feedback considerations. Such a derivation shows that the assumption of pins 2 and 3 at the same potential, though not exactly true, helps us in deriving results in a simplified way.

8.9 TERMINAL QUESTIONS

1) Design an amplifier using op amp 741C for a gain of –20 for an input of 0.5 V and an output current of 5 mA.

2) Identify the circuit given below and determine the amount of output current. What changes should be made in the circuit so that output current is doubled without changing the gain of the amplifier?



3) Design an amplifier using op amp 741C for a gain +19. If the input voltage of 0.5 V is to be amplified with an output current of 5 mA, determine the value of the load resistor.

4) Design a two-channel amplifier with gains –8 and –17.

5) Design a differentiating circuit the output of which is twice the derivative of the input signal.

6) Design an integrating circuit the output of which is one-fifth the integral of the input signal.

8.10 SOLUTIONS AND ANSWERS

SAQs

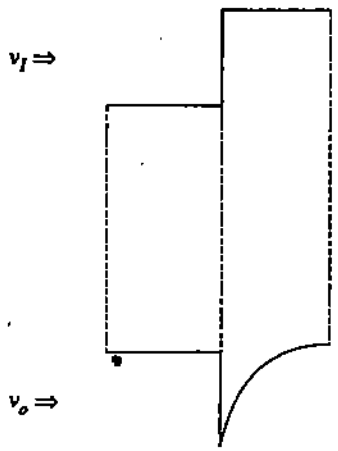
1. The output voltage is $-V_{SAT}$. (Note that the gain of the amplifier is –10. With +2 V input, the output should be –20 V. However, the output cannot be greater than $+V_{SAT}$ and less than $-V_{SAT}$. Therefore the output is $-V_{SAT}$ which is approximately –13 V.)

2. This is a non-inverting amplifier and its gain is $1 + R_F/R_I$. With $R_F = 75\,k\Omega$ and $R_I = 15\,k\Omega$, the gain of the amplifier is 6.

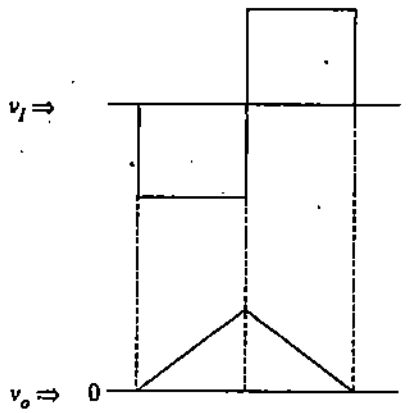
3. The circuit is for an inverting adder. The output voltage is

$$V_O = -\frac{70\ k\Omega}{10\ k\Omega}\ (5 - 3 + 1)V = -7 \times 3 = -21\,V$$

4. The output waveform is as given below.



5. The output waveform is as given below.



TQs

1) Choose the value of $R_I = 10\,k\Omega$. Therefore, for $A_{CL} = 20$,

$R_F = -A_{CL}R_I = 200\,k\Omega$.

Now $I = 0.5\ V/10\,k\Omega = 0.05\,mA$.

$I_O = I + I_L = 5\,mA = 0.05\,mA + I_L$

Or $I_L = (5 - 0.05)\,mA = 4.95\,mA$.

Now $I = V_O/R_L = 10\ V/R_L = 4.95\,mA$.

Or $R_O = 10\ V/4.95\,mA = 2.02\,k\Omega$.

Therefore, the required design is $R_I = 10\,k\Omega$, $R_F = 200\,k\Omega$, and $R_L = 2\,k\Omega$. Use $\pm 15\,V$ power supply.

2) The given circuit is for an inverting amplifier with gain = –4.5. The output voltage is –4.5 V.

Now $I_O = I + I_L = 1\,V/10\,k + 4.5\,V/5\,k\Omega$

$= 0.1\,mA + 0.9\,mA = 1\,mA$.

For doubling the output current without changing the gain of the amplifier, I_L should be = 1.9 mA.

Therefore, R_L = 4.5 V/1.9 mA = 2368 Ω.

Thus, the value of R_L should be reduced from 5 kΩ to 2368 Ω.

3) The (+) sign with gain +19 means that a non-inverting amplifier is desired the gain of which is $1 + R_F/R_I$. It means that R_F/R_I should be 18. Choose R_I = 10 kΩ, then R_F = 180 kΩ. The output voltage is V_O = 19 × 0.5 V = 9.5 V.

Now $I_O = I + I_L$ = 5 mA = 0.5 V/10 kΩ + I_L

or I_L = (5 − 05) mA = 4.95 mA.

or $R_L = V_O/I_L$ = 9.5 V/4.95 mA = 1919 Ω.

Thus the required design is R_I = 10 kΩ, R_F = 180 kΩ, and R_L = 1919 Ω or ≈ 2 kΩ.

4) This is a two input inverting adder. Choose R_{I1} for channel-1 with gain −17. Therefore, R_F = 170 kΩ which is common to both the inputs. To find R_{I2} for the channel-2, we have R_F/R_{I2} = −8. Or R_{I2} = 170 kΩ/8 = 21.25 kΩ.

Thus the required design is R_{I1} = 10 kΩ, R_{I2} = 21.25 or ≈ 20 kΩ. R_F = 170 kΩ, and choose R_L = 5 kΩ (as no current requirement is stated).

5) Basic differentiator output is $V_O = -R_F C_I dv_I/dt$. Given is $R_F C_I$ = 2. Choose C_I = 1 μF, then R_F = 2 MΩ so that $R_F C_I$ = 2.

Thus with C_I = 1 μF and R_F = 2 MΩ, the output will be twice the derivative of the input signal.

6) Basic integrator output is $V_O = -\frac{1}{R_I C_F}\int V_I dt$

For the output to be one-fifth of the integral of the input, $R_I C_F$ should be = 5. Therefor, choose C_F = 1 μF, then R_I = 5 MΩ so that $R_I C_F$ = 5. Thus, with R_I = 5 MΩ and C_F = 1 μF, the output of the basic integrator will be one-fifth of the integral of the input signal.

UNIT 9 LINEAR ICs—AMPLIFIERS AND VOLTAGE REGULATORS

Structure

9.1 INTRODUCTION

In the Units 7 and 8, linear IC op amps were described in detail basically because they find large scale applications in the electronic circuitry. There are several other widely used special purpose linear ICs. The description of all such ICs available in the market is beyond the scope of this unit. However, a few but most popular have been selected for coverage in this unit.

Small signal amplifiers amplify voltages giving at the load larger and amplified voltages. However, the power amplifiers or large signal amplifiers supply to their current operated loads a large signal current. Such loads are like speakers and motors. The operational amplifier is essentially a small signal amplifier which amplifies voltage. The current capability of op amps is also limited. The maximum current that can be obtained in case of general purpose op amp 741C with $R_L = 0$ is 25 mA. This current will obviously decrease with increase in R_L. In several applications, like audio systems, much higher current is required which cannot be supplied by general purpose op amps. Thus the loads like speakers and motors cannot be driven directly by the output of op amps. To boost the current one has to use power amplifiers based on either transistors or specialised ICs which are now commonly available in the market. In this unit, a special purpose power amplifer IC LM380, which is quite commonly used in audio systems, will be described.

Another linear IC which is quite popular now a days for its use in almost all kinds of power supplies is the voltage regulator. A voltage regulator is one that gives a constant voltage regardless of changes in the load current. An excellent performance voltage regulator can be designed using an op amp, zener diode, two resistors, and one or more transistors. All these components and some others were integrated first by Fairchild Semiconductor Division in 1968 to give a voltage regulator. Further advancement in the IC technology greatly improved voltage regulators. Currently a variety of three-terminal fixed voltage regulators for several positive and negative voltages and adjustable voltage regulators for a range of positive and negative voltages are available in the market. In this unit, 7800 and 7900 series of fixed positive and negative voltage regulator ICs, and LM317 and LM337 series of adjustable positive and negative voltage regulator ICs will be described.

Objectives

After studying this unit, you should be able to:

- draw the pin-out and block diagrams of IC LM380,
- use IC LM380 as an audio power amplifier with fixed, enhanced and variable gains,
- draw the pin-out diagrams of voltage regulators ICs of 7800, 7900, LM317 and LM337 series,
- choose an appropriate voltage regulator for your application,
- design a voltage regulation circuit for a fixed positive or negative, and adjustable positive or negative output voltages,
- using ICs of 7800, 7900 and LM317 and LM337 series,
- use a voltage regulator as a current source of desired value.

9.2 POWER AMPLIFIER IC LM380

The IC LM380 is a power audio amplifier manufactured by National semiconductor. It is an integration on a single chip of a pnp emitter follower, differential amplifier, common emitter and quasi-complementary emitter follower. The minimum power delivered by it to a load of 8 Ω is 2.5 W (rms). This makes it highly suitable for consumer electronics and other applications.

9.2.1 Characteristics of LM380

1) It has internally fixed gain of 50.
2) Output of LM380 is automatically selfcentred to one-half of the supply voltage.
3) Output is also short circuit proof.
4) It has an internal thermal limiting arrangement and therefore there is no need to use a separate heat sink.
5) Its input stage allows input signals to be ac coupled or direct coupled to either of the inputs with reference to the ground.
6) It can work on a wide range of supply voltage from 5 to 22 V.
7) It has a bandwidth of 100 kHz when used with 2 W_{rms} power output and 8 Ω load.
8) It has a sufficiently large peak current capability with a maximum of 1.3 A.
9) Total harmonic distortion is as low as 0.2%.
10) It is available in standard dip package.

9.2.2 Pin-out and Block Diagram

LM380 is a 14-pin IC with standard DIP package. Its pin-out diagram is shown in Fig.9.1. The central three pins on both sides of the package (pins 3, 4, and 5 on the left, and pins 10, 11 and 12 on the right sides) are connected to a copper lead frame so as to work as a heat sink. Note also that pin 2 is a non-inverting input and pin 6 is inverting input and the output is taken from pin 8. A capacitor of a few microfarads should be connected between the bypass pin 1 and the ground pin 7 to decouple the input stage from the supply voltage. Internally fixed voltage gain of 50 can be changed by external circuitry as explained later. Fig.9.2 shows the block diagram of LM380. The asterisk indicates ground heat sink pins.

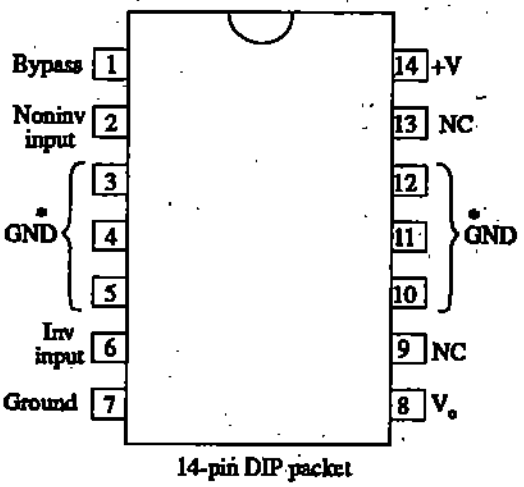


Fig.9.1: Pin-out diagram of the IC LM380 power audio amplifier.

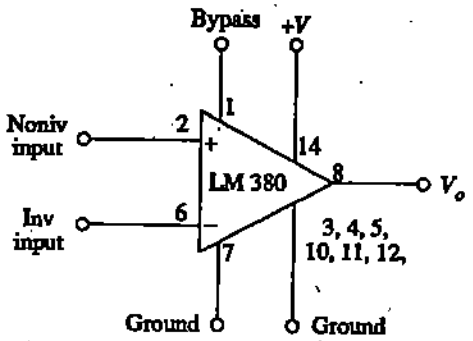


Fig.9.2: Block diagram of the IC LM380.

9.2.3 Fixed Gain Audio Amplifier

Simplest circuit using LM380 is that of an audio power amplifier shown in Fig.9.3. Because of the characteristics of LM380 outlined in section (9.2.1) and as is clear from the circuit, only a few components are externally required for use with this IC. Either of the inverting and non-inverting inputs of LM380 can be used. If the non-inverting input pin 2 is used, then the inverting input pin 6 may be either left open or connected to the ground directly or through a resistor or capacitor. If the inverting pin 6 is used, then the non-inverting input pin 2 is connected to ground directly or through a resistor or capacitor. The bias supply should be decoupled, in either case, by connecting a capacitor of 0.1 μF between supply pin 14 and the ground. If working in rf sensitive area, then an RC combination is also used between output pin 8 and ground, as shown in Fig.9.3, to avoid unwanted oscillations in the range of 5 to 10 MHz.

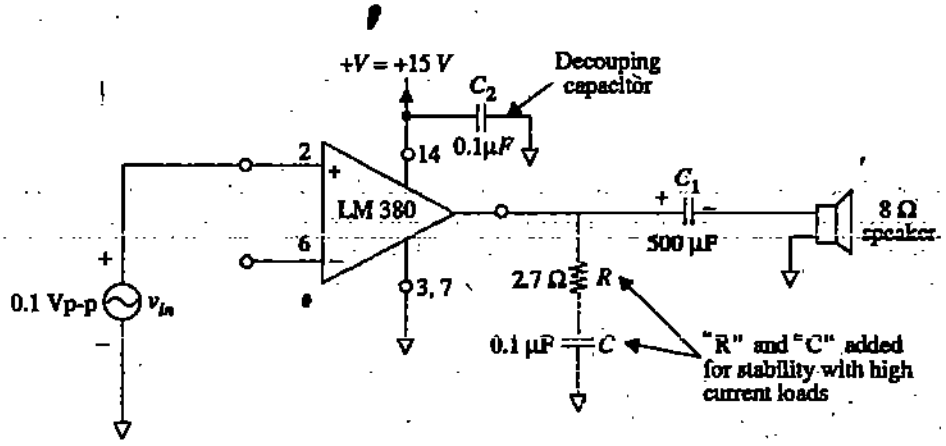


Fig.9.3: Audio power amplifier circuit using the IC LM380.

9.2.4 Higher and Variable Gain Amplifier

As stated earlier, the gain of LM380 is internally fixed at 50. However, it can be changed and made variable by using some external components. By making use of positive feedback the gain of LM380 can be increased to a gain as high as 300. Fig.9.4 shows a circuit using LM380 in its inverting configuration and designed for a gain of 200. Fig.9.5 shows a circuit designed for a variable gain upto 50 using a potentiometer between two inputs of the IC.

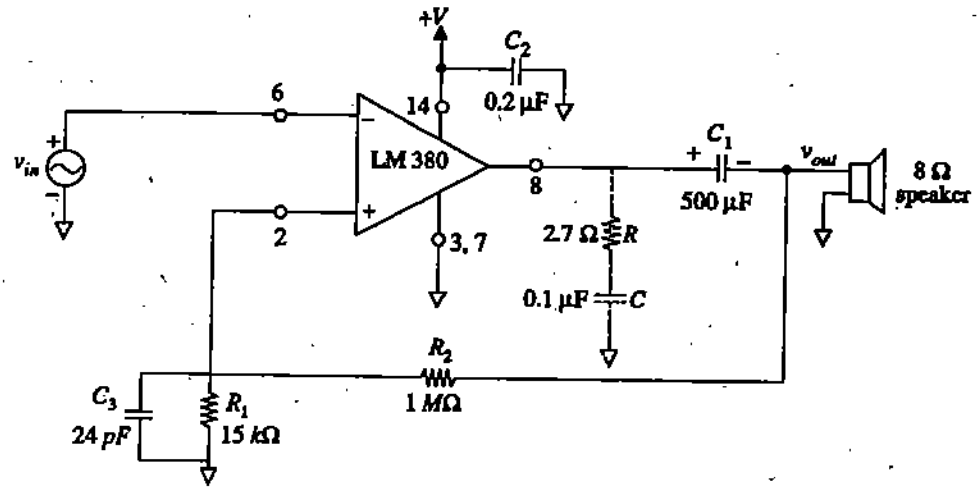


Fig.9.4: The IC LM380 power audio amplifier with a gain of 200 using positive feedback.

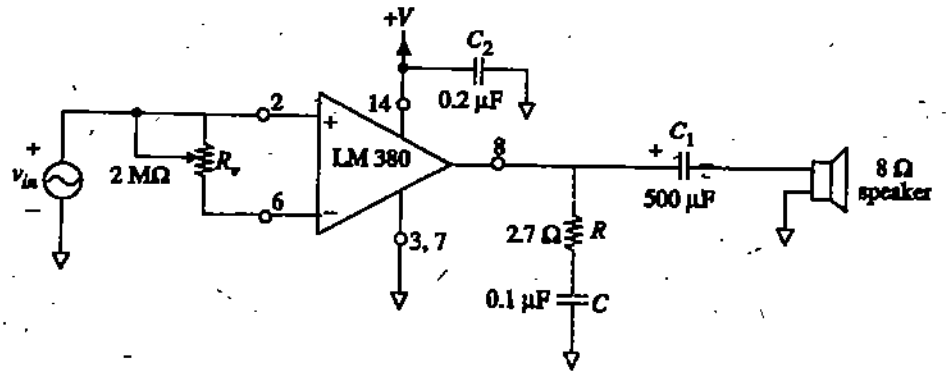


Fig.9.5: The IC LM380 power audio amplifier with a variable gain upto 50.

SAQ 1

What is the main difference between small signal amplifier and large signal or power amplifier?

9.3 VOLTAGE REGULATOR ICs

There are several types of voltage regulator ICs. Fixed output voltage regulators with positive or negative output are available for several fixed standard voltages between ±5 V and ±24 V. The voltage of the adjustable output voltage regulators with positive or negative output can be adjusted between ±1.2 V to ±37 V. The voltage regulator ICs with output currents of 0.1 A to 10 A are also available. Most regulators are three-pin devices while some special regulators are multi-pin devices.

9.3.1 Dropout Voltage

The instantaneous voltage at the input of an IC regulator must always be greater than the dc output voltage of the regulator by a value typically equal to 0.5 V to 3 V even during the low point on the input ripple voltage. In case of 7800 series of the IC voltage regulators this value is 2 V. This voltage is known as dropout voltage or headroom.

The μA7815 is a voltage regulator with a fixed positive voltage output of 15 V. Suppose a power supply, unregulated output of which is connected to the input of the μA7815, has a capacitor filter and a ripple voltage of 2 V. As shown in Fig.9.6, the minimum load voltage from the power supply which is minimum input voltage to the regulator is given by

$$V_{I\,\min} = V_O + \text{dropout voltage} \qquad (9.1)$$

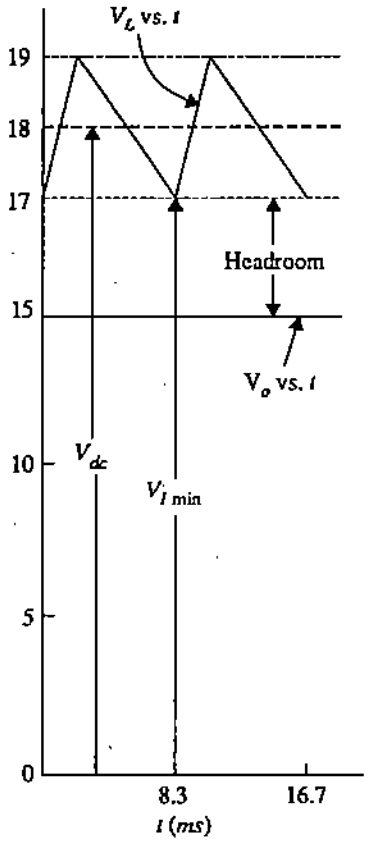


Fig.9.6: The dropout voltage.

where $V_{I\,\min}$ is the minimum input voltage to the regulator, V_O is regulated voltage output from the regulator. Thus

$$V_{I\,\min} = 15\,\text{V} + 2\,\text{V} = 17\,\text{V}.$$

Therefore, the dc voltage output of the power supply feeding the regulator should be at least 18 V (17 V + half the ripple voltage, i.e. 1 V in this example). The dropout voltage or headroom should not be too large either. A higher dc voltage fed by the power supply to the regulator wastes more heat in the regulator.

SAQ 2

Will you use a fixed voltage regulator IC giving it too much headroom?

9.3.2 Self Protection Circuits

There is internal circuitry to protect these devices from load currents exceeding the limiting values. If the load current exceeds the limiting value specified by the manufacturer, then the load current is automatically limited until the overload current is removed. And also, these regulators sense whether heat sinking is proper or not. If the internal temperature of the regulator exceeds 150 to 175°C, it shuts down its

operation. Once the fault in heat sinking is removed, the regulator starts functioning again.

9.3.3 Performance Parameters

There are four performance parameters associated with voltage regulators. These are line or input regulation, load regulation, temperature stability and ripple rejection. The input regulation is the change in the output voltage for a change in the input voltage and is measured as a percentage of output voltage. The load regulation is the change in the output voltage for a change in the input voltage. It is also measured as a percentage of the output voltage. Temperature stability is the change in the output voltage per unit change in the temperature and is measured in mV/°C. Ripple rejection is the ratio of peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage and is expressed in decibels (dB). For better regulations, the values of input regulation, load regulation and temperature stability should be smaller, and the value of ripple rejection should be higher.

SAQ 3

For a voltage regulator IC, define ripple rejection.

9.3.4 Fixed Voltage Regulators

The IC 7800 series of voltage regulators is for fixed positive voltage output with several voltage options from 5 to 24V. They have three pins—input, output and common ground. With proper heat sinking, they can deliver currents greater than 1A. The package type and pin connections are shown in Fig.9.7. Standard application circuit for the voltage regulators is shown in Fig.9.8. The Capacitor C_I is needed if the regulator is located much away from the power supply filter, while C_O, though not required, improves the transient response of the regulator.

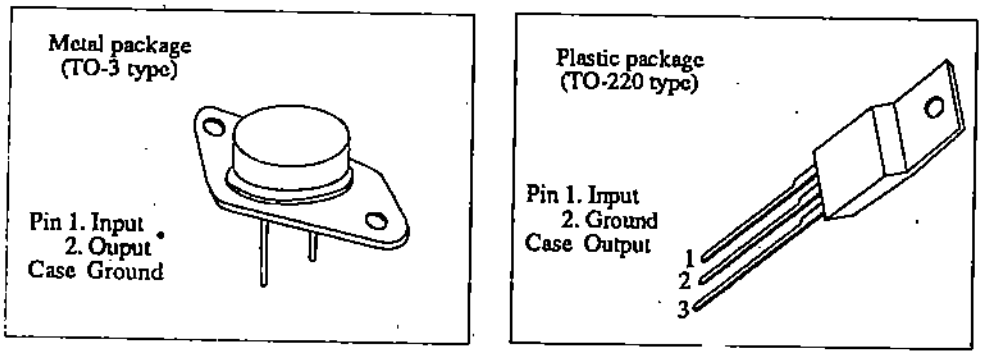


Fig.9.7: Package types and pin connections for the 7800 series ICs.

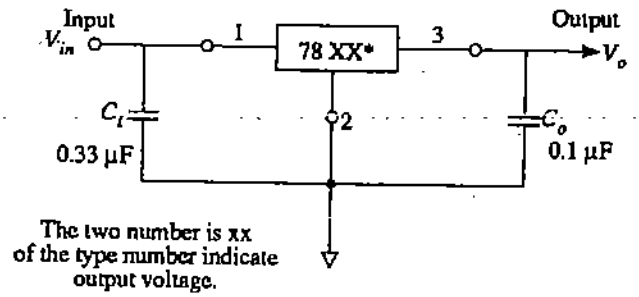


Fig.9.8: Standard application circuit for 7800 series ICs.

The IC 7800 series regulators can also be used as current sources. Consider the circuit of Fig.9.9 in which the 7805 is being used as a current source of 0.25 mA. The current supplied to the load resistor R_L is given by

$$I_L = \frac{V_R}{R} + I_Q \tag{9.2}$$

where I_Q is the quiscent current and its typical value is equal to 4.3 mA for the IC 7805. From Fig.9.9, V_R is the voltage drop across R which is the output voltage of the regulator. Therefore, $V_R = V_{23} = 5$ V. With $R = 20\ \Omega$, $V_R/R = 0.25$ A. Thus

$$I_L = 0.25\,\text{A} + 4.3\,\text{mA} \approx 0.25\,\text{A}$$

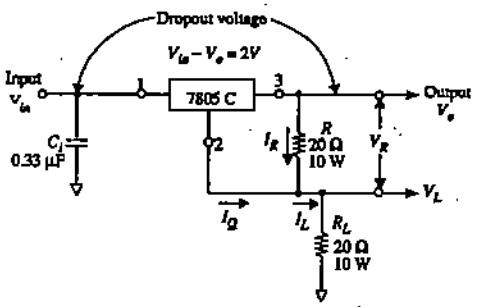


Fig.9.9: The IC 7805 as a current source.

The current $I_L = 0.25$ A is flowing through the load resistor R_L of 20Ω producing a voltage drop across R_L equal to $V_L = I_L.R_L = 5$V. The output voltage with reference to the ground is

$$V_O = V_R + V_L \tag{9.3}$$
$$= 5\text{V} + 5\text{V} = 10\text{V}.$$

With 2 V dropout voltage in case of the IC 7805, the minimum input voltage required is 12 V. Thus, we have a current source of 0.25 A. The amount of load current can be controlled by the choice of the value of R. However, the amount of a minimum input voltage required depends upon the value of R_L and the dropout voltage.

The IC 7900 series is of fixed negative voltage regulators. These are complements to the IC 7800 series fixed voltage regulators. They are also available in the same range in which the 7800 ICs are available and have two extra option of −2 and −5.2 V. The package types and the pin-out diagram for the IC 7900 series are shown in Fig.9.10.

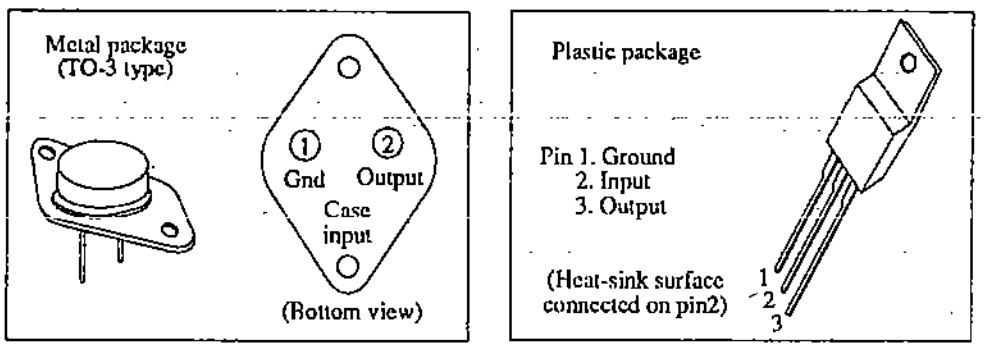


Fig.9.10: Package types and pin connections for the 7900 series ICs.

9.3.5 Adjustable Voltage Regulator

The pin connections of four standard package regulators are shown in Fig.9.11.

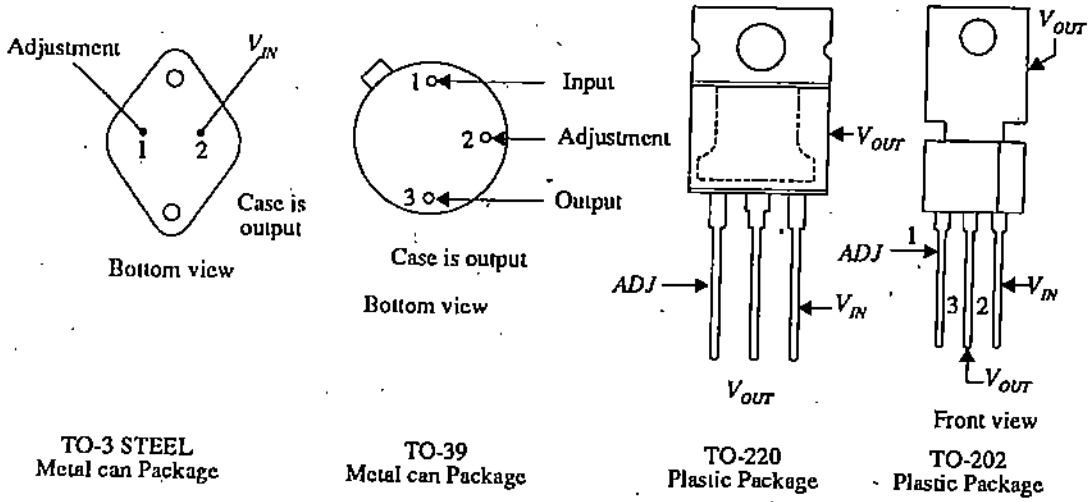


Fig.9.11: Standard package types and pin connections for the LM317 series ICs.

A typical connection diagram for using these ICs is shown in Fig.9.12. A 240Ω resistor R_1 is connected between the output and adjustment pins to conduct a current of $I_1 = V_{REF}/R$ through R_1. Since the reference voltage is constant, therefore I_1 is also constant for the value of R_1. This resistor is known as current set or programme resistor as it sets the current I_1. A small but fixed value of current also flows out of the adjustment pin through the output set resistor R_2. The maximum value of the current I_{ADJ} is 100 μA. Thus the output voltage is

$$V_O = R_1 I_1 + (I_1 + I_{ADJ})\, R_2$$

$$= I_1 (R_1 + R_2) + I_{ADJ}\, R_2$$

$$= \frac{V_{REF}}{R_1} (R_1 + R_2) + I_{ADJ}\, R_2$$

$$= V_{REF}\left(1 + \frac{R_2}{R_1}\right) + (100\ \mu A)\, R_2 \qquad (9.4)$$

$$= V_{REF}\left(1 + \frac{R_2}{R_1}\right) \qquad (9.5)$$

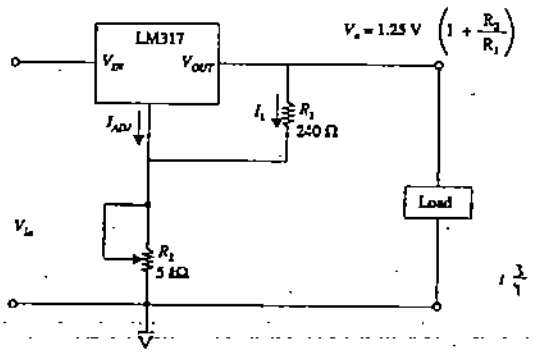


Fig.9.12: A connection diagram for the IC LM317.

The second term is ignored as it is very small (Maximum I_{ADJ} = 100 μA). Thus any desired value of the regulated output voltage can be obtained by changing R_2. The current set resistor R_1 which is normally 240Ω is connected directly to the regulator output pins rather than near the load for good load regulation. The dropout voltage

for the LM317 is 3V. So the lower point on the input voltage should be at least 3V above the regulated output voltage.

The bypass capacitors C_1 (0.1 μF) and C_2 (1 μF tantalum) are connected as shown in Fig.9.12. While C_1 minimises the problems caused by long leads between the rectifier and the regulator, C_2 improves transient response. Any ripple voltage from the rectifier will be reduced by a factor of 1000 if R_2 is bypassed by a 10 μF electrolytic capacitor. While using external capacitor, it becomes quite often necessary to provide additional protection by connecting diodes D_1 and D_2 as shown in Fig.9.13 to prevent the capacitors from discharging through low current points into the regulator. However, the diodes are not needed if the output is less than 25 V and the bypass capacitors are of values less than 25 μF.

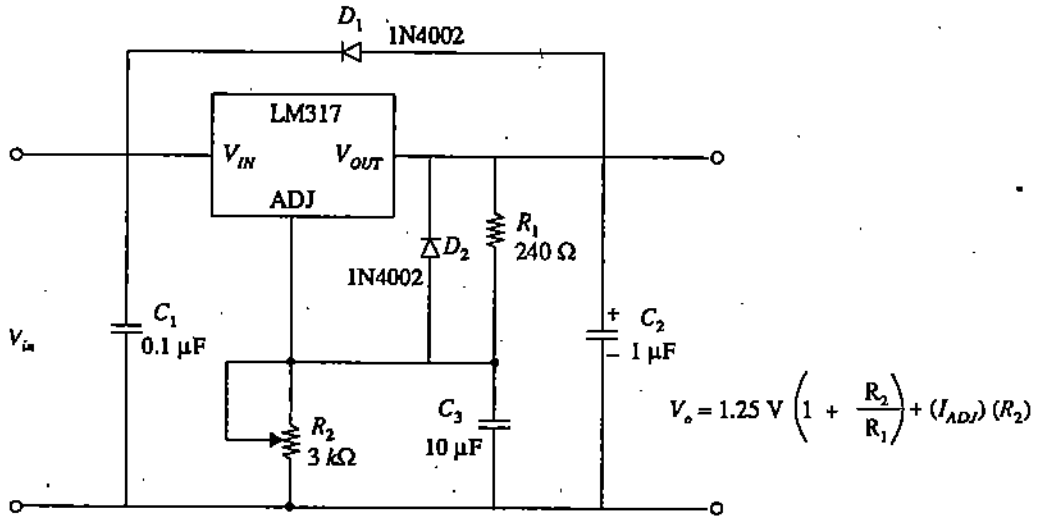


Fig.9.13: Use of capacitors and protective circuit for the IC LM317.

The IC LM337 series of adjustable voltage regulators is the complement of the IC LM317 series devices. They are also available in the same range of voltages and currents as shown in Table 9.2. The package types and pin connections are shown in Fig.9.14. The adjustable regulators operate in the same way as the positive adjustable regulators with the difference that R_1 is 120 Ω.

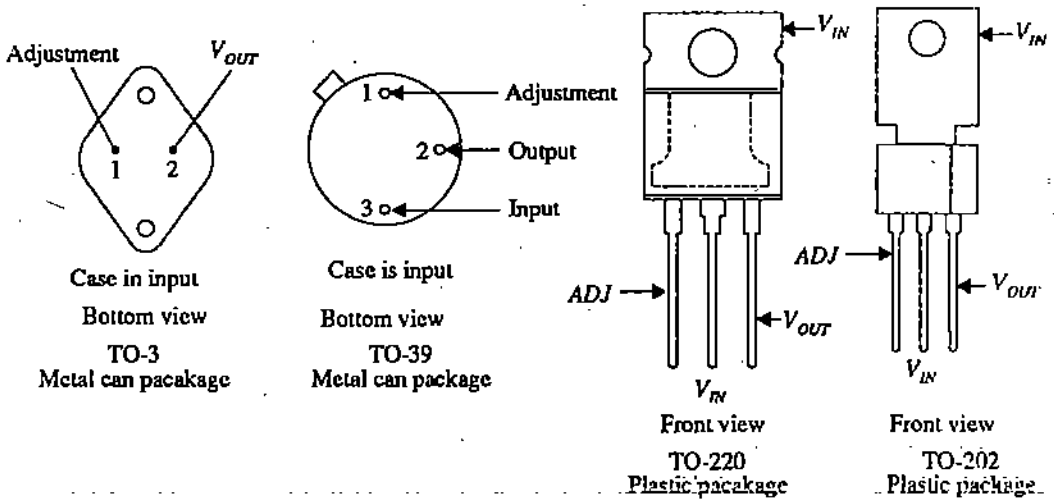


Fig.9.14: Standard package types and pin connections for the LM337 series of ICs.

Example 9.2

Using an IC LM317, design an adjustable voltage regulator for an output voltage of 5 to 20V.

Solution:

Using equation (9.4) and $R_1 = 240\,\Omega$, we get

$$5\,V = 1.25\left(1 + \frac{R_2}{240\,\Omega}\right) + (100\ \mu A)\ R_2$$

$$= 1.25 + R_2\left(\frac{1.25}{240} + 10^{-4}\right)$$

$$= 1.25 + R_2\ (5.3 \times 10^{-3})$$

$$R_2 = \frac{3.75}{(5.3)\ (10^{-3})}$$

$$= 708\ \Omega$$

Similarly, for 20 V, the value of R_2 is

$$20 = 1.25\left(1 + \frac{R_2}{240}\right) + (10^{-4})\ R_2$$

$$R_2 = \frac{18.75}{(5.3)\ (10^{-3})}$$

$$= 3538\,\Omega.$$

Thus to obtain an adjustable voltage regulator for the voltage range from 5 to 20 V, we need to vary the value of R_2 from 708 Ω to 3538 Ω. Therefore, connect a carbon potentiometer of 5 kΩ as variable R_2. As stated earlier, connect C_1 of 0.1 μF, C_2 of 1 ΩμF and C_3 of 10 μF for improved ripple rejection.

SAQ 5

What is reference voltage for the ICs LM317 and LM337?

SAQ 6

What is dropout voltage in case of the ICs LM317 and LM337?

9.4 SUMMARY

- Though general purpose op amps can be used satisfactorily in certain applications, yet it is easier and cheaper to use some special purpose linear ICs commercially available in the market.
- Power amplifiers supply large signal current to current operated loads like speakers and motors. The IC LM380 manufactured by National Semiconductor is a very popular linear IC used in audio amplifiers. It can deliver a minimum of 2.5 W (rms) power to a load of 8 Ω. The gain of the IC LM380 is internally fixed at 50. However, it can be increased upto 300 and varied upto 50 by using positive feedback through external circuitry.
- The 7800 series of the voltage regulator IC is used for getting fixed positive regulated voltages in the range of 5 to 24 V. These ICs require a dropout voltage of 2 V, that is the input voltage to the regulator should be at least 2 V more than the regulated voltage required even at the lowest point at the input ripple. Two capacitors C_I and C_O are used if the regulator is away from the power supply and to improve transient response respectively.
- The 7900 series of ICs is the complement of the IC 7800 series and is for fixed negative regulated voltages. These ICs work in the same way as the 7800 series ICs works.

- The IC 7800 series voltage regulators can also be used as current source of desired values as stated in the text. Apart from the regulator IC, only two resistors are required for this application.
- The LM317 series of ICs is for adjustable positive regulated voltages. The voltage range available from the series is from 1.2V to 57V. The dropout voltage for these ICs is 3V. Apart from the IC, a 240Ω resistor is used between the output and adjustment pins to set the current and another resistor used is a carbon potentiometer which sets the adjustable output voltage. As stated in the text, three capacitors are also used with the IC for improved performance and ripple rejection.
- The IC LM337 series is the complement of the IC LM317 and is for adjustable negative regulated voltages. These ICs function in the same way as the ICs of the LM317 series function. The only difference here is that the current set resistor is of 120Ω rather than 240 as in the case of LM317.

9.5 TERMINAL QUESTIONS

1) What are the important characteristics of the IC LM380?

2) The output of a power supply with a capacitor filter is having a ripple voltage of 3V. What should be the dc voltage output of this power supply if the regulated output desired is of 10V? What is the number code of the regulator chosen by you for this purpose?

3) A voltage regulator IC has a ripple rejection of 60 dB. If the ripple voltage at the input of the regulator is 5V, then what is value of the ripple at the regulator output?

4) Design an adjustable voltage regulator using IC LM317 for a voltage range of 8 to 16V.

9.6 SOLUTIONS AND ANSWERS

SAQs

1. Small signal amplifiers are basically voltage amplifiers which give at the load larger amplified voltages, while the large signal or power amplifiers supply large-signal currents to current-operated loads like speakers and motors. This is the main difference between the small-signal and large signal or power amplifiers.
2. No, because it will waste more heat in the regulator.
3. Definition given in section (9.3.3).
4. In case of ICs of 7800 series, pin 1 is input, pin 2 is ground and pin 3 is output. Whereas, in case of ICs of 7900 series, pin 1 is ground, pin 2 is input and pin 3 is output.
5. It is the fixed voltage developed between the output and adjustment pins and is 1.25V.
6. 3V.

TQs

1) Characteristics are listed in section (9.2.1).

2) Choose the regulator IC 7810. This IC has a dropout voltage of 2V. Therefore, $V_{I\,min}$ = 10V + 2V = 12V. But the given power supply has a ripple of 3V. Hence the dc output of the power supply should be $V_{I\,min}$ +half the ripple voltage, that is 12 + 1.5 = 13.5V.

3) Ripple rejection $= 20 \log \frac{\text{ripple at input}}{\text{ripple at output}} = 60\,\text{dB}$ (given)

It means that log term should be equal to 3. It would be so when numerator in the log term is 1000 and denominator is 1. Hence, the input and output ripples are in the ratio of 1000:1. Since the input ripple is of 5 V, the output ripple would be 5 mV.

[Another way is to put the value of input ripple, and solve the equation for the output ripple].

4) Follow the steps given in the example 9.2 in the text. The value of R_2 for 8 V is 1273 Ω, and that for 16 V is 2783 Ω. Therefore, a carbon potentiometer of 3 kΩ should be used.

NOTES

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Block

4

DIGITAL ELECTRONICS

BLOCK 4 DIGITAL ELECTRONICS

In the previous three Blocks we dealt with analog electronics in which the inputs and output are analog (continuously varying) signals. In this block, we will be studying about digital circuits where the signals are discrete.

The origin of digit was in the caves, thousands of years before written-history when man learned to count on the fingers (digits). The basic number names, are therefore, known as digits. There are different numbering systems followed in digital electronics. In Unit 10 you will be introduced to some of the important number systems used. We will learn how to convert numbers from one system to another. We will discuss binary number and some mathematical operations using them.

In Unit 11 we will introduce some of the circuits that are able to operate on binary numbers to perform a logical function. These circuits are called electronic gates. Also you will be familiarised with boolean algebra which is used in digital systems. After having learned about different types of gates you will be introduced to flip flop which can be built using gates.

In Unit 12 we will study about counters which are used for counting the digital pulses and registers which are used to store binary information. Many digital systems include some form of memory, where data can be held on a permanent or a temporary basis. There are different types of memories used in a digital system. We will learn about semiconductor memories in the this Unit. Data from the physical world are usually analog in form and continuous in time. The digital computer or processor operates with numbers and discontinuous data. To utilize the digital processor in the solution or control of physical problems it requires devices to sample the analog data and code it in digital form or to perform reverse processing and decoding in conversion of processed information back to analog form. Therefore, in Unit 12 we have discussed analog to digital converter and their counterpart digital to analog converter.

In Unit 13 we will come across many testing, measuring and indicating instruments like CRO, electronic voltmeter, powermeter etc. It would help the students to familiarize themselves with these instruments.

minutes, or more accurately 10 hour 39 minutes 50 seconds). As is clear from the examples above, the accuracy of the value of an analog quantity generally depends upon the judgement of the observer.

Many number systems are being used in digital technology. Most common amongst them are decimal, binary, octal, and hexadecimal systems. We are most familiar with the decimal number system, because we use it everyday. In this unit we shall describe these number systems, the conversion of a number from one system to another, and finally binary arithmetic. This unit is intended to provide the first step in our understanding of digital electronics.

In the next unit you will be introduced to some of the gates which are fundamental in digital electronics. There you will be familiarised with Boolean algebra which is a mathematical method used in the design of digital systems.

Objectives

After studying this unit, you should be able to

- write binary number and convert it into its decimal equivalent and a decimal number into its binary equivalent,
- explain octal number system, understand octal counting, convert an octal number into its decimal and binary equivalents and decimal and binary numbers into their octal equivalents,
- explain hexadecimal number system, understand hex counting, convert hex number into its decimal, binary and octal equivalents and decimal, binary and octal numbers into their hex equivalents,
- write BCD code and convert a decimal number into its equivalent BCD code and vice versa,
- understand ASCII code,
- learn addition, subtraction, multiplication and division using binary numbers.

10.2 BINARY NUMBER SYSTEM

First let us consider the familiar decimal system. In this system there are ten distinct and different digits (0, 1, 2, 3, 4, 5, 6, 7, 8, and 9). For magnitudes greater than 9 the convention is to arrange digits in rows starting with the most significant on the left and concluding with the least significant on the right. The significance is determined by what is called the 'weighting' of a digit. Thus arises the concept of 'tens', 'hundreds', 'thousands', etc. For example $3458 = (3 \times 10^3) + (4 \times 10^2) + (5 \times 10^1) + (8 \times 10^0)$. Each digit is one of the symbols 0 to 9 and is multiplied by a power of ten, depending upon the position of digit. Thus decimal numbers are said to have a base of ten and the multiplying powers 10^0, 10^1, 10^2, 10^3 etc. are called 'weight' or 'positional values'.

In the binary number system (base of 2), there are only two digits: 0 and 1 and the place values are 2^0, 2^1, 2^2, 2^3 etc. Binary digits are abbreviated as bits. For example 1101 is a binary number of 4 bits (i.e., it is a binary number containing four binary digits.)

A binary number may have any number of bits. Consider the number 11001.011. Note the binary point (counterpart of decimal point in decimal number system) in this number. The bit on the extreme right is called least significant bit (LSB) and the bit on the extreme left is called most significant bit (MSB). Each bit has its positional value as shown in Fig. 10.1.

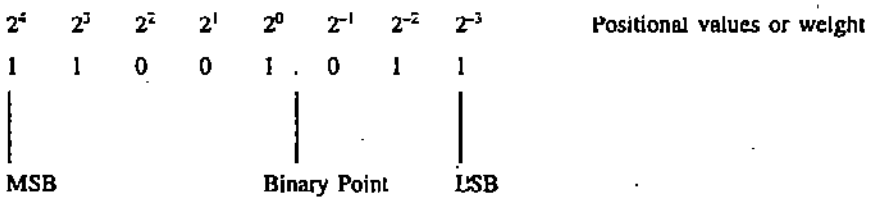


Fig. 10.1: Binary number: showing positional values (weight) of each bit.

The bits on the left of the binary point are positive powers of 2 and bits on the right of binary point are negative powers of 2. The decimal equivalent of this number is found by summing the products of each bit and its positional value as follows:

$$11001.011_2 = (1 \times 2^4) + (1 \times 2^3) + (0 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) + (0 \times 2^{-1}) + (1 \times 2^{-2}) + (1 \times 2^{-3})$$

$$= 16 + 8 + 0 + 0 + 1 + 0 + 0.250 + 0.125$$

$$= 25.375_{10}.$$

Note that to avoid confusion the subscripts 2 and 10 are written with the numbers to indicate the base of the appropriate number system in which the number is expressed.

Any number can be expressed in binary form in the usual way as shown in Table 10.1.

Table 10.1: Counting in Binary System.

2^3	2^2	2^1	2^0	Binary Number	Decimal Number
0	0	0	0	0000	0
0	0	0	1	0001	1
0	0	1	0	0010	2
0	0	1	1	0011	3
0	1	0	0	0100	4
0	1	0	1	0101	5
0	1	1	0	0110	6
0	1	1	1	0111	7
1	0	0	0	1000	8
1	0	0	1	1001	9
1	0	1	0	1010	10
1	0	1	1	1011	11
1	1	0	0	1100	12
1	1	0	1	1101	13
1	1	1	0	1110	14
1	1	1	1	1111	15

From this Table, note that 4 binary digits are required to do counting upto 15_{10}. Thus if the number of bits is n, then we can go upto 2^n counts and the largest decimal number represented will be $2^n - 1$. For example, in the above case, n = 4 and therefore, the largest decimal number represented is $2^4 - 1 = 15_{10}$. To write the next higher number in Table 10.1, we need an additional column for the next power of the base i.e. 2^4.

SAQ 1

What is the largest decimal number that can be represented using 10 bits?

The advantage of binary system is that it has made the job of designing the digital circuitry very easy because only two distinct states or levels of voltages have to be handled. For example, 'ON' state of a bulb may be represented by the bit '1' and 'OFF' state by '0'. In terms of voltages, 0 V or a 'LOW' voltage may represent bit '0' and 5 V or a 'HIGH' voltage may represent bit '1'. Actually, it is not necessary also to have precise voltages assigned to each bit. In analog system the exact value of voltage is very important which makes the design of accurate analog circuitry very difficult. However, in digital systems exact value of voltage is not important because a voltage of 3.9 V means the same thing as a voltage of 4.4 V or 5 V. This aspect will be dealt with in Unit 12.

Let us now see how binary numbers can be converted into equivalent decimal form and vice-versa.

10.2.1 Binary to Decimal Conversion

From the example discussed above it is clear that a binary number can be converted into its decimal equivalent by simply adding the weights of various positions in the binary number which have bit 1. For example, consider the conversion of 100011.101_2.

$$1 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1 . 1 \quad 0 \quad 1$$

$$2^5 + 0 + 0 + 0 + 2^1 + 2^0 + 2^{-1} + 0 + 2^{-3}$$

$$= 32 + 2 + 1 + 0.5 + 0.125$$

$$= 35.625_{10}$$

Let us take up another example of conversion of 11100111.0101_2.

$$11100111.0101$$

$$2^7 + 2^6 + 2^5 + 0 + 0 + 2^2 + 2^1 + 2^0 + 0 + 2^{-2} + 0 + 2^{-4}$$

$$= 128 + 64 + 32 + 4 + 2 + 1 + 0.250 + 0.0625$$

$$= 231.3125_{10}.$$

Consider the following examples.

$$1111.00 = 15$$

$$11110.0 = 30$$

$$111100.0 = 60$$

From these examples it is clear that if the binary point is shifted towards right side, then the value of the number is doubled.

Now consider the following examples.

$$111.100 = 7.5$$

$$11.1100 = 3.75$$

$$1.11100 = 1.875$$

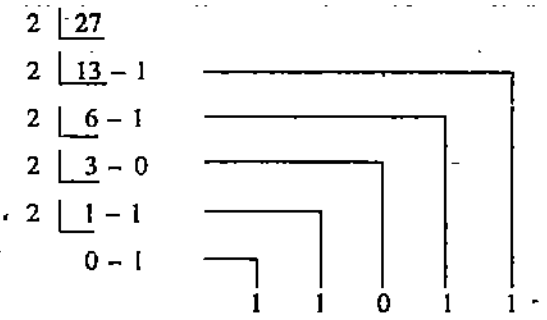
From these examples it is clear that if the binary point is shifted towards the left side, then the value of the number is halved.

SAQ 2

Convert 1011.101 into its decimal equivalent.

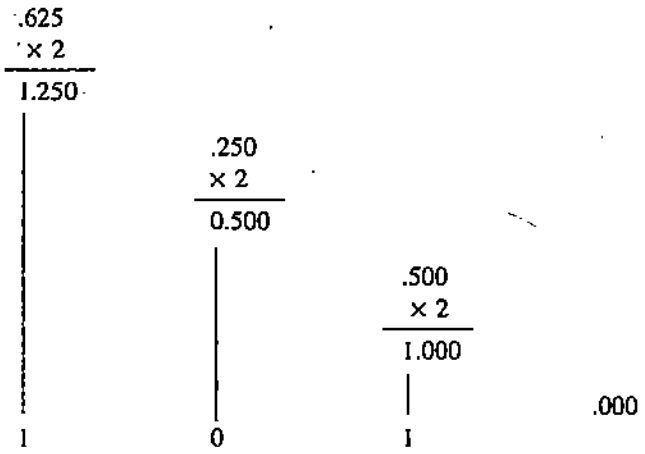
10.2.2 Decimal to Binary Conversion

A decimal number is converted into its binary equivalent by its repeated divisions by 2. The division is continued till we get a quotient of 0. Then all the remainders are arranged sequentially with first remainder taking the position of LSB and the last one taking the position of MSB. Consider the conversion of 27 into its binary equivalent as follows.



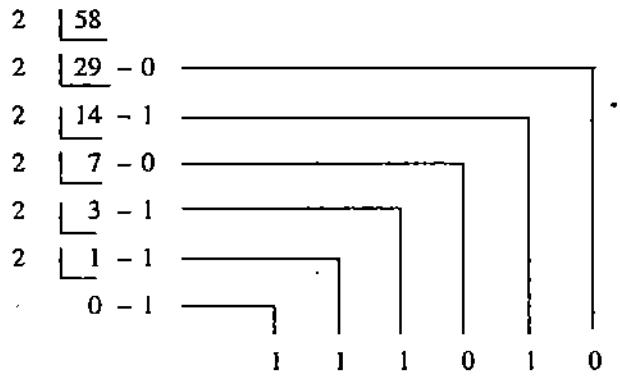
Thus $27_{10} = 11011_2$.

If the number also has some figures on the right of the decimal point, then this part of the number is to be treated separately. Multiply this part repeatedly by 2, After first multiplication by 2, either 1 or 0 will appear on the left of the decimal point. Keep this 1 or 0 separately and do not multiply it by 2 subsequently. This should be followed for every multiplication. Continue multiplication by 2 till you get all 0s after the decimal point or upto the level of the accuracy desired. This will be clear from the following example. Consider the conversion of 27.625_{10} into its binary equivalent. We have already converted 27 into its binary equivalent which is 11011_2. Now for the conversion of 0.625, multiply it by 2 repeatedly as follows:

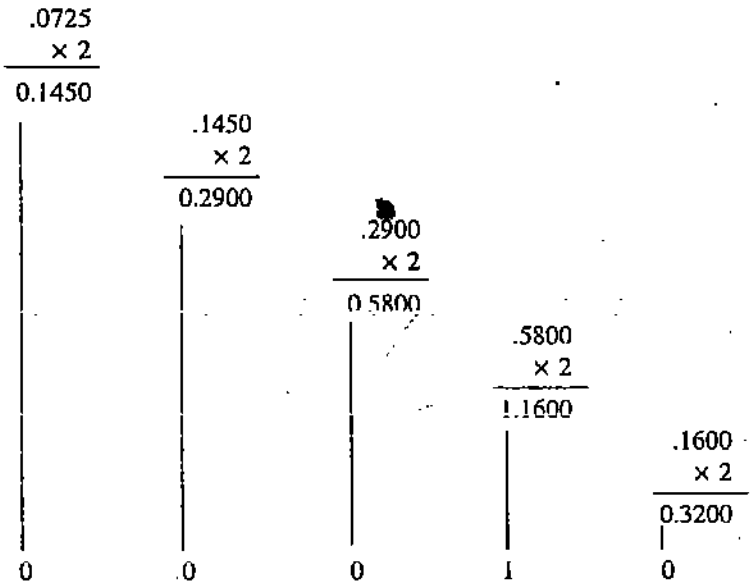


Thus $27.625_{10} = 11011.101_2$.

Let us try another example, conversion of 58.0725_{10} into binary. Split this number in two parts, i.e. 58 and .0725 and convert them into binary separately as described above.



Now take up the conversion of .0725



Thus $58.0725_{10} = 111010.00010_2$

SAQ 3

What is the binary equivalent of 37.75_{10}?

Representing numbers in binary is very tedious since binary numbers often consist of a large chain of 0's and 1's. Imagine the length of the binary equivalent of a 10 digit decimal number !!. So, convenient shorthand forms for representing the binary numbers are developed such as octal system and hexadecimal system. With these number systems long strings of 0's and 1's can be reduced to a manageable form. Let us see what these systems are.

10.3 OCTAL NUMBER SYSTEM

The octal number system has base-8, that is there are 8 digits in this system. These digits are 0, 1, 2, 3, 4, 5, 6, and 7. The weight of each octal digit is some power of 8 depending upon the position of the digit. This is explained in Fig. 10.2.

8^4	8^3	8^2	8^1	8^0	8^{-1}	8^{-2}	Weights
1	0	6	2	7 .	4	5	Octal Number
MSD				Octal Point		LSD	

Fig. 10.2: Octal number: showing positional values (weights) of each digit.

Octal number does not include the decimal digits 8 and 9. If any number includes decimal digits 8 and 9, then the number can not be an octal number.

Now let us see how counting is done in octal system. You are familiar with the counting in decimal system. In decimal system there are 10 digits from 1 to 9 hence the counting in such system is done as in Table 10.2.

Table 10.2: Counting in decimal system.

0	10	20	30	40	50	60	70	100	110	....	170
1	11	21	31	41	51	61	71	101	111		
2	12	22	32	42	52	62	72	102	112		
3	13	23	33	43	53	63	73	103	113		
4	14	24	34	44	54	64	74	104	114		
5	15	25	35	45	55	65	75	105	115		
6	16	26	36	46	56	66	76	106	116		
7	17	27	37	47	57	67	77	107	117		
8	18	28	38	48	58	68	78	108	118		
9	19	29	39	49	59	69	79	109	119	....	179

In the same style, counting can be done in octal system as shown in Table 10.3.

Table 10.3: Counting in octal system.

0	10	20	30	40	50	60	70	100
1	11	21	31	41	51	61	71	101
2	12	22	32	42	52	62	72	102
3	13	23	33	43	53	63	73	103
4	14	24	34	44	54	64	74	104
5	15	25	35	45	55	65	75	105
6	16	26	36	46	56	66	76	106
7	17	27	37	47	57	67	77	107

In the octal counting, if n is the number of digits then the total number of counts is 8^n. The largest decimal number represented by an octal number having n digits is $8^n - 1$. Thus with $n = 4$, the total number of counts is $8^4 = 4096$ and the largest decimal number represented is $4096 - 1 = 4095_{10}$.

SAQ 4

Can the number 128.96 be an octal number?

SAQ 5

What is the largest decimal number that can be represented by a three digit octal number?

10.3.1 Octal to Decimal Conversion

As has been done in case of binary numbers, an octal number can be converted into its decimal equivalent by multiplying the octal digit by its positional value. For example,

$$\begin{aligned} 126.25_8 &= (1 \times 8^2) + (2 \times 8^1) + (6 \times 8^0) + (2 \times 8^{-1}) + (5 \times 8^{-2}) \\ &= 64 + 16 + 6 + 0.25 + 0.078 \\ &= 86.328_{10} \end{aligned}$$

Let us convert 36.48 into decimal number.

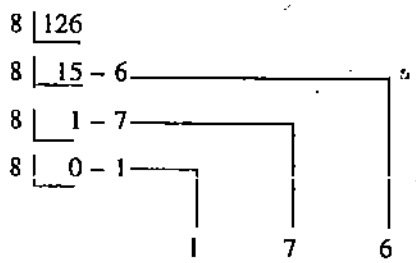
$$\begin{aligned} 36.4_8 &= 3 \times 8^1 + 6 \times 8^0 + 4 \times 8^{-1} \\ &= 24 + 6 + 0.5 \\ &= 30.5_{10} \end{aligned}$$

SAQ 6

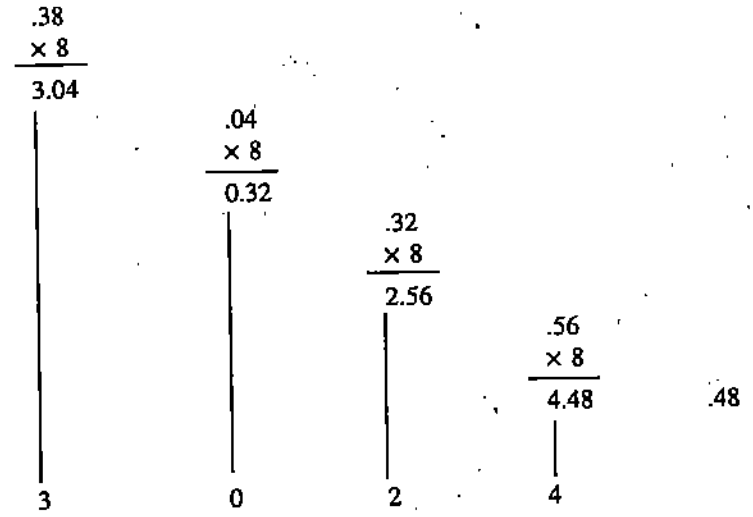
What is the decimal equivalent of 37.2_8?

10.3.2 Decimal to Octal Conversion

A decimal number can be converted by repeated division by 8 into equivalent octal number. This method is similar to that adopted in decimal to binary conversion.
If the decimal number has some digits on the right of the decimal point, then this part of the number is converted into its octal equivalent by repeatedly multiplying it by 8. The process is same as has been followed in binary number system. Consider the conversion of 126.38_{10} into its decimal equivalent. Split it into two parts, that is 126 and .38



Now the conversion of .38 is as follows:



Thus $126.38_{10} = 176.3024_8$

SAQ 7

What is the octal equivalent of 15.250_{10}?

10.3.3 Octal to Binary Conversion

In the octal number system the highest octal digit i.e. 7 can be expressed as a 3-bit binary number. Therefore, all the octal digits have to be represented by a 3-bit binary number. The binary equivalent of each octal digit is shown in Table 10.4. The main advantage of the octal number system is the easiness with which any octal number can be converted into its binary equivalent.

Table 10.4: Binary equivalent of each octal digit.

Octal digit	3-bit binary equivalent
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Using this conversion of octal digit into 3-bit binary number, any octal number can be converted into its binary equivalent by simply replacing each octal digit by a 3-bit binary number. For example, conversion of 567_8 into its binary equivalent is:

$$567_8 = 101\ 110\ 111$$
$$= 101110111_2$$

Thus $567_8 = 101110111_2$.

Another example:

Conversion of 672.27_8 into its binary equivalent.

$$672.27_8 = 110\ 111\ 010.010\ 111$$
$$= 110111010.010111_2$$

Thus $672.27_8 = 110111010.010111_2$

SAQ 8

Represent 10027.12_8 in binary number.

10.3.4 Binary to Octal Conversion

A binary number can be converted into its octal equivalent by first making groups of 3-bits starting from the LSB side. If the MSB side does not have 3 bits, then add 0s to make the last group of 3 bits. Then by replacing each group of 3 bits by its octal equivalent, a binary number can be converted into its binary equivalent. For example, consider the conversion of 1100011001_2 into its octal equivalent as follows:

1100011001_2 = 1 100 011 001

= 001 100 011 001 [As the MSB side does not have 3 bits, we have added two 0's to make the last group of 3 bits]

= 1 4 3 1

= 1431_8

Thus $1100011001_2 = 1431_8$

SAQ 9

What is the octal equivalent of 10010_2?

10.4 HEXADECIMAL NUMBER SYSTEM

The hexadecimal number system has base-16, that is it has 16 digits (Hexadecimal means '16'). These digits are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F. The digits A, B, C, D, E, and F have equivalent decimal values 10, 11, 12, 13, 14, and 15 respectively. Each Hex (hexadecimal is popularly known as hex) digit in a hex number has a positional value that is some power of 16 depending upon its position in the number. This is illustrated in Fig. 10.3.

16^3	16^2	16^1	16^0	16^{-1}	16^{-2}	Weights
1	2	4	A	B	9	Hex number
MSD			Hex Point		LSD	

Fig. 10.3: Hexadecimal number: showing positional values (weight) of each digit.

The relationship of hex digits with decimal and binary numbers is given in Table 10.5. Note that to represent the largest hex digit we require four binary bits. Therefore, the binary equivalent of all the hex digits have to be written in 4-bit numbers.

Table 10.5: Binary and Decimal equivalent of each Hex Digit.

Hex digit	Decimal equivalent	4-bit Binary equivalent
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
A	10	1010
B	11	1011
C	12	1100
D	13	1101
E	14	1110
F	15	1111

While doing counting in hex number system if n is the number of hex digits then counting can be done upto 16^n counts and the largest decimal number represented by a hex number is $16^n - 1$. The hex counting is shown in Table 10.6.

Table 10.6: Counting in Hexadecimal system.

0	10	20	10	40	...	90	A0	B0	C0	D0	E0	F0	100
1	11	21	31	41	...	91	A1	B1	C1	D1	E1	F1	
2	12	22	32	42	...	92	A2	B2	C2	D2	E2	F2	
3	13	23	33	43	...	93	A3	B3	C3	D3	E3	F3	
9	19	29	39	49	...	99	A9	B9	C9	D9	E9	F9	
A	1A	2A	3A	4A	...	9A	AA	BA	CA	DA	EA	FA	
B	1B	2B	3B	4B	...	9B	AB	BB	CB	DB	EB	FB	
C	1C	2C	3C	4C	...	9C	AC	BC	CC	DC	EC	FC	
D	1D	2D	3D	4D	...	9D	AD	BD	CD	DD	ED	FD	
E	1E	2E	3E	4E	...	9E	AE	BE	CE	DE	EE	FE	
F	1F	2F	3F	4F	...	9F	AF	BF	CF	DF	EF	FF	

SAQ 10

What is the number next to $835F_{16}$?

SAQ 11

What is the largest decimal number represented by a 3-digit hex number?

10.4.1 Hex to Decimal Conversion

Hex to decimal conversion is done in the same way as in the cases of binary and octal to decimal conversions. A hex number is converted into its equivalent decimal number by summing the products of the weights of each digit and their values. This is clear from the example of conversion of $514.AF_{16}$ into its decimal equivalent.

$$\begin{aligned} 514.AF_{16} &= 5 \times 16^2 + 1 \times 16^1 + 4 \times 16^0 + 10 \times 16^{-1} + 15 \times 16^{-2} \\ &= 1280 + 16 + 4 + 0.625 + 0.0586 \\ &= 1300.6836_{10}. \end{aligned}$$

Another example:

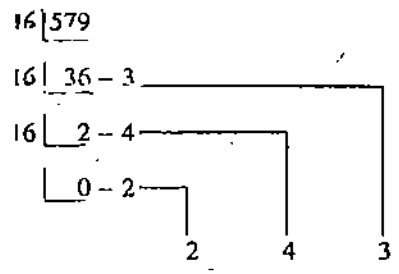
$$\begin{aligned} 3BE.1A_{16} &= 3 \times 16^2 + 11 \times 16^1 + 14 \times 16^0 + 1 \times 16^{-1} + 10 \times 16^{-2} \\ &= 768 + 176 + 14 + 0.0625 + 0.0391 \\ &= 958.1016_{10}. \end{aligned}$$

SAQ 12

What is decimal equivalent of $1BE2_{16}$?

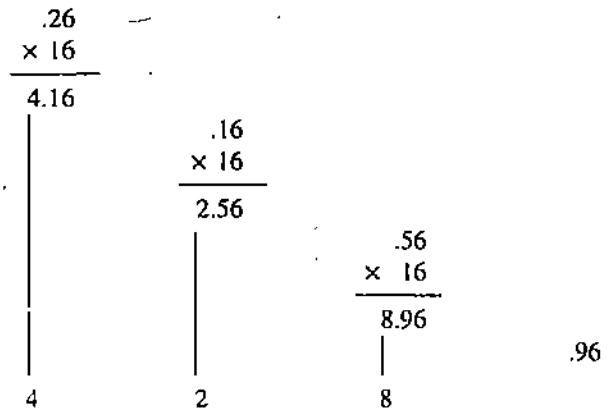
10.4.2 Decimal to Hex Conversion

A decimal number is converted into hex number in the same way as a decimal number is converted into its equivalent binary and octal numbers. The part of the number on the left of the decimal point is to be divided repeatedly by 16 and the part on the right of the decimal point is to be repeatedly multiplied by 16. This will be clear from the examples of conversion of 579.26_{10} into hex equivalent. Split the number into two parts 579 and .26.



Thus $579_{10} = 243_{16}$.

Now .26 is converted into hex number as follows:



Thus $579.26_{10} = 243.428_{16}$.

SAQ 13

What is the hex equivalent of 37_{10}.

10.4.3 Hex to Binary Conversion

As in octal number system, a hex number is converted into its binary equivalent by replacing each hex digit by its equivalent 4-bit binary number. This is clear from the following example:

$$BA6_{16} = B \quad A \quad 6$$
$$= 1011 \quad 1010 \quad 0110$$
$$= 101110100110_2$$

SAQ 14

What is the binary equivalent of $6F10_{16}$?

10.4.4 Binary to Hex Conversion

By a process that is reverse of the process described in section 10.4.4 above, a binary number can be converted into its hex equivalent. Starting from the LSB side, group the binary number bits into groups of four bits. If towards the MSB side, the number of bits is less than four then add zeros on the left of the MSB so that the group of four is complete. Replace each group by its equivalent hex digit. This is clear from the following example:

$$1001101110_2 = 0010 \quad 0110 \quad 1110$$
$$= 2 \quad 6 \quad E$$
$$= 26E_{16}.$$

SAQ 15

What is the hex equivalent of 1100101010011111_2?

10.4.5 Hex to Octal Conversion

Each digit of the hex number is first converted into its equivalent four bit binary number. Then the bits of the equivalent binary number are grouped into groups of three bits. Then each group is replaced by its equivalent octal digit to get the octal number. For example:

$$\begin{aligned} 5AF_{16} &= 0101 \quad 1010 \quad 1111 \\ &= 010110101111 \\ &= 010 \quad 110 \quad 101 \quad 111 \\ &= 2 \quad 6 \quad 5 \quad 7 \\ &= 2657_8 \end{aligned}$$

SAQ 16

What is the octal equivalent of $5A9_{16}$?

10.4.6 Octal to Hex Conversion

For octal to hex conversion, just reverse the process described in section 10.4.6 above. This is clear from the following example:

$$\begin{aligned} 5457_8 &= 101 \quad 100 \quad 101 \quad 111 \\ &= 1011 \quad 0010 \quad 1111 \\ &= B \quad 2 \quad F \\ &= B2F_{16}. \end{aligned}$$

This method can also be applied to hex to decimal and decimal to hex conversions. For example consider the conversion of $3C_{16}$ into its decimal equivalent:

$$\begin{aligned} 3C_{16} &= 0011 \quad 1100 \\ &= 111100_2. \end{aligned}$$

Check the conversion.

$$\begin{aligned} 3C_{16} &= 3 \times 16^1 + C \times 16^0 \\ &= 3 \times 16^1 + 12 \times 16^0 \\ &= 48 + 12 \\ &= 60_{10}. \\ 111100_2 &= 2^5 + 2^4 + 2^3 + 2^2 \\ &= 32 + 16 + 8 + 4 \\ &= 60_{10}. \end{aligned}$$

Thus $3C_{16} = 111100_2 = 60_{10}$.

SAQ 17

What is the hex equivalent of 327_8?

10.5 CODES

So far you have learnt about binary, octal and hexadecimal number system. For any number system with a base B and digits N_0 (LSB), N_1, N_2, ... N_m (MSB), the decimal equivalent N_{10} is given by

$$N_{10} = N_m \times B^m + ... N_3 \times B^3 + N_2 \times B^2 + N_1 \times B^1 + N_0 B^0 \qquad (10.1)$$

You have also observed that a number in any system can be written in the binary form. A number code is a relationship between the binary digits and the number represented. Thus, all number systems are codes and the decimal equivalent is given by Eq. (10.1). But there are other relationships or codes that relate decimal numbers and groups of binary digits that do not obey Eq. (10.1) These relationships are called codes. We will now discuss some of the important codes used in digital work.

10.5.1 BCD Code

In BCD (BCD stands for binary coded decimal) code, each digit of a decimal number is converted into its four bit binary equivalent. The largest decimal digit is 9, therefore the largest binary equivalent is 1001. This is illustrated as follows:

$$951_{10} = 1001\ \ 0101\ \ 0001$$
$$= 100101010001_{BCD}.$$

Remember that the conversion of a decimal number into its binary equivalent and BCD equivalent leads to two different numbers. For example:

$$158_{10} = 0001\ \ 0101\ \ 1000$$
$$= 101011000_{BCD}.$$

$158_{10} = 10011110_2$ (obtained by repeated division method).

Thus we see that it is quite easy to convert from decimal to BCD and from BCD to decimal. It is much easier to convert from BCD to decimal than from straight binary to decimal, because we only have to count upto 9 in binary to do so. However, it takes more bits to represent a number in BCD than in binary.

A BCD number is converted into its decimal equivalent by the reverse process. For example:

$$1010101110010_{BCD} = 0001\ \ 0101\ \ 0111\ \ 0010$$
$$= 1\ \ 5\ \ 7\ \ 2$$
$$= 1572_{10}.$$

Although the main function of a computer is to perform arithmetic operations, it also processes messages and information in a language that uses letters of the alphabet (e.g. English) and data of other kinds. Computers operate by coding letters of the alphabet, other symbols, and data into binary form. The code used for this purpose is ASCII code about which you will study now.

10.5.2 ASCII Code

The word ASCII is an acronym of American Standard Code for Information Interchange. This is the alphanumeric code most widely used in computers. The alphanumeric code is one that represents alphabets, numerical numbers, punctuation marks and other special characters recognised by a computer. The ASCII code is a 7-bit code representing 26 English alphabets, 0 through 9 digits, punctuation marks, etc. A 7-bit code has $2^7 = 128$ possible code groups which are quite sufficient. A partial ASCII code listing is shown in Table 10.6.

Table 10.6: Some of the ASCII codes for numbers, alphabets and other common symbols.

$A_6A_5A_4$						$A_3A_2A_1A_0$
010	011	100	101	110	111	
SP	0	@	P		p	0000
!	1	A	Q	a	q	0001
"	2	B	R	b	r	0010
#	3	C	S	c	s	0011
$	4	D	T	d	t	0100
%	5	E	U	e	u	0101
&	6	F	V	f	v	0110
'	7	G	W	g	w	0111
(	8	H	X	h	x	1000
)	9	I	Y	i	y	1001
*	:	J	Z	j	z	1010
+	;	K		k		1011
,	<	L		l		1100
−	=	M		m		1101
.	>	N		n		1110
/	?	O		o		1111

The code is $A_6A_5A_4A_3A_2A_1A_0$. For example, A has $A_6A_5A_4$ of 100 and an $A_3A_2A_1A_0$ of 0001. Therefore, its ASCII code is

100 0001 = A.

The ASCII code for a is 110 0001.

SAQ 18

What is the ASCII code of SHARMA?

10.6 BINARY ARITHMETIC

Digital computers can perform arithmetic operations using only binary numbers. We will learn how to add, subtract, multiply and divide binary numbers. We will first review this in the familiar decimal system and apply the same ideas to binary system.

10.6.1 Addition

Let us recall the addition in decimal numbers. Suppose we want to add 563 and 146. We start adding the digits in the least significant column. We get,

```
  563
+ 146
-----
    9   (no carry to the next column)
-----
```

Next, the digits of the second column are added and we get,

```
  563
 +146
 ----
  09   (carry 1 to the next column)
 ----
```

In this case 6 + 4 gives 0, with a carry 1 to the next column. Then the digits of the last column and the 'carry' from the previous column are added. We get,

```
  563
  146
  1    ..... carry from previous column
 ----
 709   (no carry)
 ----
```

Addition of binary numbers can be carried out in a similar way by the column method. But before we do this, we need to discuss four simple cases. We known in the decimal number system, 3 + 6 = 9 symbolizes the combining of ... with ..... to get a total of ..... Let us now discuss the four simple cases.

Case 1: When nothing is combined with nothing, we get nothing. The binary representation of this is 0 + 0 = 0.

Case 2: When nothing is combined with ., we get. Using binary numbers to denote this gives 0 + 1 = 1.

Case 3: Combining . with nothing gives. The binary equivalent of this is 1 + 0 = 1.

Case 4: When we combine . with ., the result is .. Using binary numbers, we symbolize 1 + 1 = 10.

The last result is sometimes confusing because of our long time association with decimal numbers. But it is correct and makes sense because we are using binary numbers. Binary number 10 stands for.. and not for ..... (ten).

To summarize our results for binary addition,

0 + 0 = 0

0 + 1 = 1

1 + 0 = 1

1 + 1 = 10

To add large binary numbers, carry into higher-order columns as is done with decimal numbers. As an example, add 10 to 10 as follows

```
  10
+ 10
----
 100
----
```

In the first column, 0 plus 0 is 0. In the second column, 1 plus 1 is 0, carry a 1. As another example, take 1 + 1 + 1. Add two of the 1's to get 10 + 1.

Adding again gives 11 as follows:

1 + 1 + 1 = 10 + 1 = 11

See another example

```
  101   first column: 1 + 0 = 1
+ 110   second column : 0 + 1 = 1
-----
 1011   third column: 1 + 1 = 10 (zero, carry one)
-----
```

Further examples are

```
   110          101.011
 + 111        + 111.110
------       ---------
  1101         1101.001
------       ---------
```

In all digital networks or computers only two binary numbers are added at a time. To add more than two numbers, first two numbers are added, then to their sum the third number is added, and so on. Therefore, we should not worry about the addition of more than two numbers. The computer can add numbers in a few microseconds or even less. You will see that the multiplication, division and subtractions are actually done by the computers by way of addition.

SAQ 19

Add the following : (a) 1010 and 1101

(b) 1011 and 1010

10.6.2 Subtraction

Binary subtraction is done in the same way as in decimal system. Let us recall the decimal subtraction, for example.

```
  56
- 49
----
   7
----
```

In this example, a 1 is borrowed from the ten's position giving 16 in the LSD. Then 16 – 9 = 7. Borrowing a 1 from the ten's position leaves 4 in place of 5. Then 4 – 4 = 0. In the same way the binary subtraction can be done.

To subtract binary numbers, we first need to discuss four simple cases.

Case 1 0 – 0 = 0

Case 2 1 – 0 = 1

Case 3 1 – 1 = 0

Case 4 10 – 1 = 1

The last result represents . . – . = . which makes sense. To subtract large binary numbers, subtract column by column, borrowing from the adjacent column when necessary. For example, in subtracting 101 from 111, we proceed as follows:

```
  111        first column :    1 – 1 = 0
- 101        second column:    1 – 0 = 1
-----
  010        third column:     1 – 1 = 0
```

Here is another example: subtract 1010 from 1101

```
 1101        first column:     1 – 0 = 1
- 1010        second column:    10 (after borrow) – 1 = 1
-----
             third column:     0 (after borrow) – 1 = 0
             fourth column:    1 – 1 = 0.
```

SAQ 20

Subtract binary 100011 from 110011.

10.6.3 Multiplication and Division

The multiplication of binary numbers is also done in the same manner as in decimal system. It is rather easier, because the multiplication table for binary has only four cases.

Case 1 $0 \times 0 = 0$

Case 2 $0 \times 1 = 0$

Case 3 $1 \times 0 = 0$

Case 4 $1 \times 1 = 1$

For example, in multiplying 1101 by 1001, we proceed as follows:

```
  1101
  1001
 ------
  1101
 0000
0000
1101
-------
1110101
-------
```

In the beginning the first partial product is written. Subsequently each partial product is written below the previous one by shifting one place towards left relative to the previous place. However, the digital circuits or computers add only two binary numbers at a time. Therefore, to the sum of first two partial products is added the third partial product. To this sum is added the third partial product to give the final sum.

The process of dividing a binary number is once again the same as followed in the decimal system. To divide 1100 by 10, we proceed as follows.

```
    110
  ------
10| 1100
   10
  ----
    10
    10
  ----
     00
```

SAQ 21

Multiply 10110 by 110.

10.7 SUMMARY

- There are mainly four number systems namely binary, octal, decimal and hexadecimal which have 2, 8, 10 and 16 digits respectively. But it is the ease in applications that decides which kind of number system should be defined and used. Every computer uses two or more of the above mentioned number systems simultaneously.
- The binary number system has only two digits: 0 and 1. A binary digit is called bit. A binary number can be converted into its equivalent octal, decimal and hex numbers as described in the text. And also octal, decimal and hex numbers can be converted into equivalent binary numbers.
- The octal number system has 8 digits: 0 through 7. An octal number can be converted into its equivalent binary, decimal and hex numbers and vice versa as described in the text.

- The hex number system has 16 digits: 0 through 9; A (10) through F (15). As in the other systems, the hex numbers can be converted as described in the text into their binary, octal and decimal equivalents and vice versa.
- It is possible to arrange sets of binary digits to represent numbers, letters of the alphabet or other information by using a given code. Some of the important codes are BCD and ASCII codes.
- In the BCD code, each decimal digit is replaced by its 4-bit binary equivalent. The conversion of BCD code into its decimal equivalent and vice versa is quite easy. Therefore, it is quite often used in computers.
- The ASCII code is the most widely used alphanumeric code. It is a 7-bit binary number and has $2^7 = 128$ possible 7-bit binary numbers which are quite sufficient to describe the capital and small letters of the alphabet, digits, punctuation marks, and other symbols.
- The fundamental arithmetic of binary addition is contained in four rules:

  1. $0 + 0 = 0$
  2. $0 + 1 = 1$
  3. $1 + 0 = 1$
  4. $1 + 1 = 0$ but 1 must be carried over to next higher (more significant) bit.

- The fundamental arithmetic of binary subtraction is contained in four rules:

  1. $0 - 0 = 0$
  2. $0 - 1 = 1$ and borrow 1 from the next more significant bit
  3. $1 - 0 = 1$
  4. $1 - 1 = 0$

- The four rules for binary multiplication are:

  1. $0 \times 0 = 0$
  2. $0 \times 1 = 1$
  3. $1 \times 0 = 1$
  4. $1 \times 1 = 0$

10.8 TERMINAL QUESTIONS

1) In the binary sequence, what is number that follows 10111?
2) What is the largest decimal number that can be expressed by 6 bits?
3) Convert 11011011010.1101_2 into its decimal equivalent.
4) Convert 372.125_{10} into its binary equivalent.
5) Convert 89.875_{10} into its binary equivalent.
6) What is the largest decimal number represented by a five digit octal number?
7) Convert 7777_8 into its decimal equivalent.
8) Convert 6789_{10} into its octal equivalent.
9) Convert 23401_8 into its binary equivalent.
10) Convert 1100110111001010_2 into its octal equivalent.
11) Add the following binary numbers 1110001 and 1010101
12) Multiply 101.1 by 11.01
13) Divide 11011 by 100

10.9 SOLUTIONS AND ANSWERS

SAQs

1. Largest decimal number $=2^n - 1$. With $n = 10$, $2^{10} - 1 = 1024 - 1 = 1023_{10}$.
2. 11.625_{10}.
3. 100101.11.
4. No. Octal numbers do not have digits 8 and 9.
5. The largest decimal number is $8^3 - 1 = 512 - 1 = 511_{10}$.
6. 31.250_{10}
7. 17.2_8.
8. $0010000000101 1.001010_2$.
9. 22_8.
10. 8360_{16}.
11. Largest decimal number $= 16^3 - 1 = 4096 - 1 = 4095_{10}$.
12. $1BE2_{16} = 1 \times 16^3 + 11 \times 16^2 + 14 \times 16^1 + 2 \times 16^0$
    $= 4096 + 2816 + 224 + 2$
    $= 7138_{10}$.
13. 25_{16}.
14. $6F10_{16} = 0110\ \ 1111\ \ 0001\ \ 0000 = 110111100010000_2$.
15. $1100101010011 11_2 = 0110\ \ 0101\ \ 0100\ \ 1111 = 654F_{16}$.
16. $5A9_{16} = 0101\ \ 1010\ \ 1001$
    $= 010\ 110\ 101\ 001$
    $= 2651_8$.
17. $3278 = 011\ \ 010\ \ 111$
    $= 0\ 1101\ \ 0111$
    $= D7_{16}$
18. SHARMA = 1010011 1001000 1000001 1010010 1001101 1000001
19. (a) 10111 (b) 10101
20. 10000.
21. 10000100.

TQs

1) 11000_2.
2) 63_{10}.
3) 1754.8125_{10}.
4) 101110100.001_2.
5) 1011001.111_2.

6) 32767_{10}.

7) 4095_{10}.

8) 15205_{8}.

9) 10011100000001_{2}.

10) 1100110111001010_2 = 001 100 110 111 001 010

= 1 4 6 7 1 2

= 146712_8.

11) 11000110

12) 10001.111

13) 110.11

UNIT 11 FUNDAMENTALS OF BOOLEAN ALGEBRA AND FLIP FLOPS

Structure

11.1 INTRODUCTION

A digital circuit is designed for a desired application by a combination of several logic gates. This application involving several logic gates may be a simple or complex one. Different users may design digital circuits by using different combinations of logic gates for the same application. In selecting one of these digital circuits for that application, it is necessary to keep in mind that the chosen digital circuit should have a minimum number of logic gates. By seeing a digital circuit, it is not obvious that a circuit is minimal or certain gates may be removed from the circuit without changing its operation. Boolean algebra provides a means by which logic circuitry may be expressed symbolically, manipulated and reduced.

In this Unit we shall learn about three basic logic gates: AND, OR, NOT and their various combinations. All digital (logic) circuits operate in the binary mode where all the inputs and outputs are predefined voltages representing binary digit either 1 or 0. It is this characteristics of the logic circuits that enables us to use boolean algebra for designing and analysing the digital systems. This area of digital circuitry is known as combinational logic where the relationship between the inputs and outputs can be precisely defined by the logic summarised in a truth table.

In the combinational logic circuits there is no memory, i.e. the output of the digital circuit does not depend upon the occurrence of a previous event. But it is very essential for more advanced digital circuits meant for storing and manipulating information to have memory. The basic memory element is a flipflop which is obtained by using NAND or NOR gates. In this Unit we shall learn about various kinds of flipflops and their operation. This area of digital circuitry is known as sequential circuits.

Objectives

After studying this unit, you should be able to

- describe the operation of AND, OR and NOT Gates and write their truth tables,
- describe the combination of gates and write the truth tables of NAND and NOR gates,
- explain as to how a timing diagram of the output of all the logic circuits is obtained,
- explain how the operation of three basic logic gates lead us to various theorems or rules used in the boolean algebra,
- write boolean theorems and use algebraic method for combinational logic,
- obtain a truth table from a give boolean expression,
- describe the operation of exclusive—OR and exclusive—NOR gates,
- design a half adder and describe its operation,
- design a full adder and describe its operation,
- design logic circuits using only NAND gates,
- describe the construction and explain the operation of the RS flipflop,
- describe the construction and explain the operation of clocked RS flipflop, D flipflop, and JK flipflop,
- obtain the timing diagrams of the outputs of flipflops.

11.2 LOGIC GATES

A logic gate is a digital circuit which has logical relationship between input and output voltages. There are three basic gates: AND, OR and NOT (also called inverter) gates. We shall now learn these gates one by one.

11.2.1 AND Gate

The AND gate can be understood by the circuit given in Fig. 11.1. In this circuit switch (s) is input and the bulb is output. Let us assign 0 to the event when the switch is open and 1 to the event when the switch is close. Similarly when the bulb does not glow we call it 0 and when the bulb glows we call it 1. With both the switches (A and B) off, the bulb (Y) does not glow.

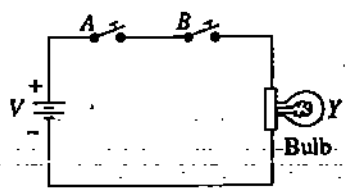


Fig. 11.1: AND gate using switches.

With one of the switches off and another switch on, once again the bulb (Y) does not glow. However, with both the switches (A and B) on, the bulb (Y) glow. Thus there are four events which can be summarised in the form of a table which is called the truth table of this circuit. This is given in Table 11.1. The switches A and B, which control the input voltage are usually called input of the truth table and Y as the output.

Table 11.1: Truth Table of AND Gate.

inputs		output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

From this table it is clear that the bulb glows (1) only when both the switches (A and B) are on (1). Stated in a different way, the output is 1 when both the inputs A and B are 1. This state of the circuit is distinct from other three states. This circuit is known as the AND gate. The symbol of AND gate is given in Fig. 11.2. It is clear from the Fig. 11.1 that if the circuit has any number of switches in series, then the output will be 1 if and only if all inputs are 1. Now for all times to come, you must remember that **for an AND gate the output is 1 if and only if all the inputs are 1.**

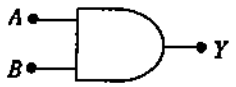


Fig. 11.2: Symbol of AND gate.

Electronically the AND gate can be realised by using two pn junction diodes as shown in the circuit of Fig. 11.3. The resistor R is used to control the current passing through the diodes. As stated above, a 0 bit is assigned 0V and a 1 bit is assigned 5V. However, such accurate values of voltage will not always be available at the output in electronic circuits. Therefore, a 0 bit is assigned a voltage range of 0 to 0.8V and a 1 bit is assigned to a voltage range of 2.8 to 5.0V. Quite often these voltage ranges are referred to a LOW and a HIGH respectively. The voltages greater than 0.8V and less than 2.8 V are indeterminate and hence not used.

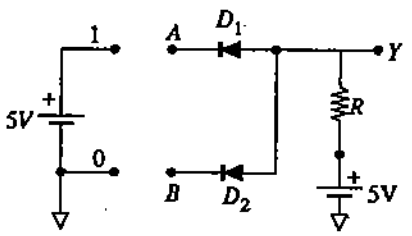


Fig. 11.3: Realisation of AND Gate using diodes.

In the circuit of Fig. 11.3 when the inputs A and B are 0, i.e. when they are connected to the 0V or ground terminal, both the diodes are forward biased with a voltage drop of 0.7V across each diode if the diodes are of Si or of 0.3V if the diodes are of Ge. Hence the output voltage is a LOW or a 0 bit. If the input A is 0 and B is 1 (i.e. 5V), the diode A is forward biased with 0.7V drop across it (assuming diode to be of Si) while the diode B is not biased (because both p and n sides of the diode are at the same voltage, 5V). Therefore the output voltage is 0.7V, i.e. a LOW or a 0 bit. Similarly, if the input A is 1 and input B is 0, the output is a 0. However, if both inputs are 1, i.e. connected to 5V, then both the sides of the diodes are at the same voltage and hence not conducting. Therefore, the output voltage is nothing but the battery voltage which is 5V, i.e. a HIGH or a 1 bit. These four cases satisfy the truth table of Table 11.1. For more input AND gate, the number of diodes may be more. The input output relationship of the AND gate is written as A.B = Y and is read as A AND B equal to Y.

Example 11.1

If the inputs A and B to the AND gate are as shown in Fig. 11.4, trace the output Y.

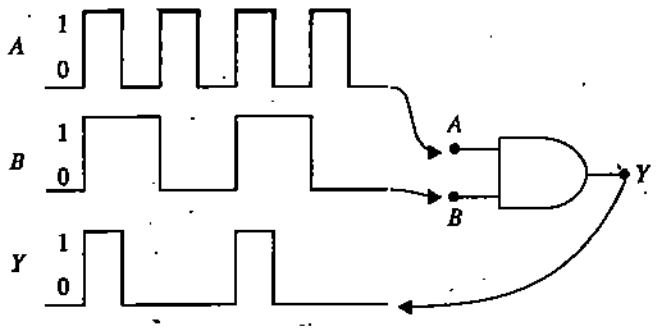


Fig. 11.4:

Solution

Recall that output of an AND gate is 1 when all the inputs are 1. If any of the inputs is 0, then the output is 0. With this understanding, the output comes out to be as shown in the trace for Y.

SAQ 1

Trace the output of an AND gate, if the inputs A and B are as shown in Fig. 11.5.

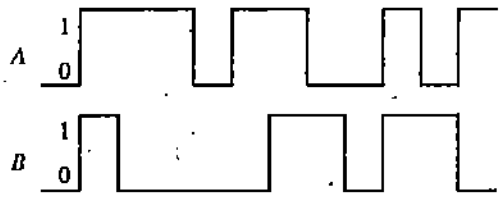


Fig. 11.5:

11.2.2 OR Gate

The OR gate operation can be understood by the circuit of Fig. 11.4. If both the switches are off, (0), the bulb does not glow (0). If one of the switches is on (1) and other is off (0), the bulb glows (1). And if both the switches are on (1), then also the bulb glows (1). These events are summarised in the truth table given in Table 11.2.

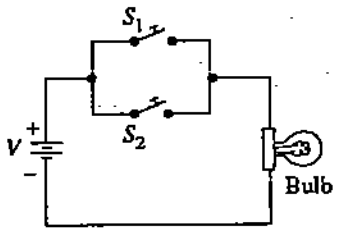


Fig. 11.6: OR gate using switches.

Table 11.2: Truth Table of OR Gate.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

It is clear from the truth table that the output of OR gate is 0 if both the inputs are 0 and the output is 1 if any one of the inputs or both the inputs are 1. If a larger number of switches are used in parallel in the circuit, then the bulb does not glow if all the switches are off, and the bulb glows if any one of the switches is on. The symbol of OR gate is given in Fig. 11.7. The OR gate operation is expressed as A + B = Y and is read as A OR B = Y.

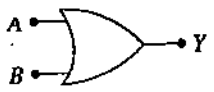


Fig. 11.7: Symbol of OR gate.

Electronically OR gate can be realised by using two pn junction diodes as shown in the circuit of Fig. 11.8. If both the inputs are 0, that is connected to the ground, then the diodes are not biased and hence no current flows through the diodes. The output is zero or a 0 bit. If the inputs to diode A is 0 and B is 1 (i.e. 5V), then the diode A is not biased and thus does not conduct, but the diode B is forward biased with a 0.7V drop across it and 4.3V drop across the resistor. Thus the output is a HIGH or a 1 bit. Similarly, if the inputs to the diode A is 1 and diode B is 0, the output is 1. When the inputs to both the diodes A and B are 1, both the diodes are forward biased, the voltage drop across the resistor R continues to be 4.3V. Hence, the output is a 1 bit. All these four cases satisfy the truth table of OR gate. A more input OR gate is obtained by using more diodes in the circuit. Analysing the truth table of OR gate, we learn that **the output is 0 if both or all the inputs are 0, and the output is 1 if at least one of the input is 1.**

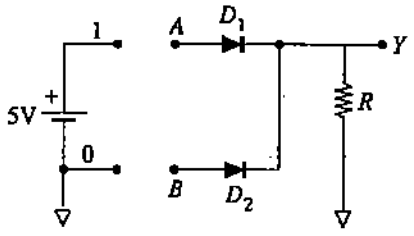


Fig. 11.8: Realisation of OR gate using diodes.

Example 11.2

If the inputs A and B to OR gate are as shown in Fig. 11.9, trace the output Y.

Recall that the output of an OR gate is 1 if any of the input is 1, and the output is 0 if all the inputs are 0. With this understanding, the output comes out to be as shown in the trace for Y.

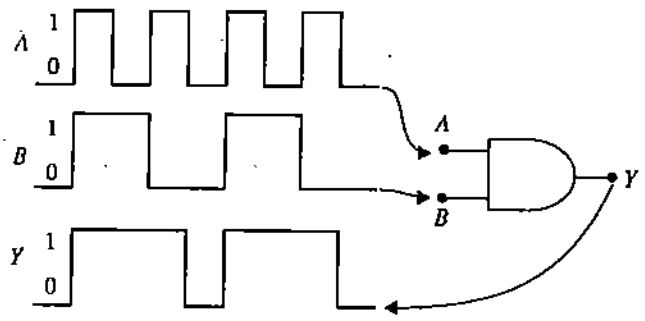


Fig. 11.9:

SAQ 2

Trace the output of an OR gate if the inputs A and B are as shown in Fig. 11.10

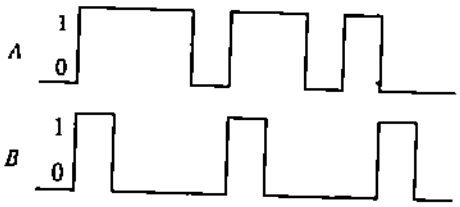


Fig. 11.10:

11.2.3 NOT Gate

The NOT gate can be understood by considering the electrical circuit shown in Fig. 11.11. Let us assign a 0 bit to the even when bulb does not glow and 1 bit to the event when bulb glows, and a 0 bit to switch off and 1 bit to switch closed. In Fig. 11.11, when switch is closed, no current will pass through the bulb and the bulb will not glow. This is because the current always flow through the least resistance path. Similarly, when the switch is open then the whole current will flow through the bulb making it glow.

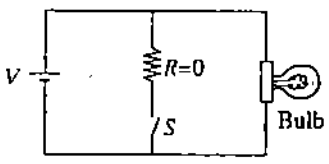


Fig. 11.11: NOT gate using a switch.

If input to the circuit is 1, the output is 0 and if the input is 0 then the output is 1. This is the NOT gate operation which is summarised in the truth table given in Table 11.3.

Table 11.3: Truth table for NOT gate.

A	Y
0	1
1	0

The NOT gate is also known as INVERTER. It has only one input. Its symbol is given in Fig. 11.12. The input-output relationship is expressed as A = Y.

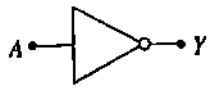


Fig. 11.12: Symbol of NOT gate.

The NOT gate can be realised using the circuit given in Fig. 11.13. The circuit uses the cutoff and saturation modes of the transistor. When the input to the circuit is a 0 bit, i.e. zero volt, no base current, I_B, flows. This means the collector current, I_C, is zero. This is cutoff mode of the transistor.

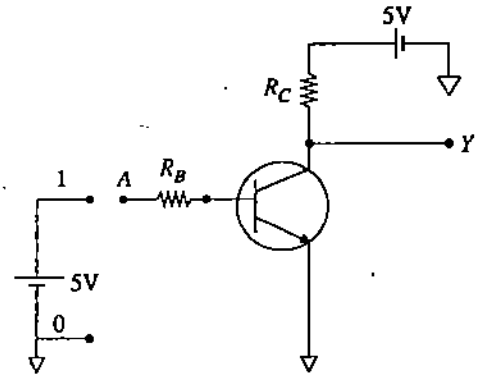


Fig. 11.13: Realisation of NOT gate using a transistor.

Therefore, the output voltage is the bias voltage of 5V indicating the output to be a 1 bit. When the input to the circuit is a 1 bit, i.e. 5V, very large I_B flows resulting in very large I_C, in fact $I_{C\,sat}$. This is the saturation mode of the transistor. This indicates that most of the bias voltage is dropped across R_C with output to be a 0 bit.

Example 11.3

If the input A to NOT gate is as shown in Fig. 11.14, trace the output Y.

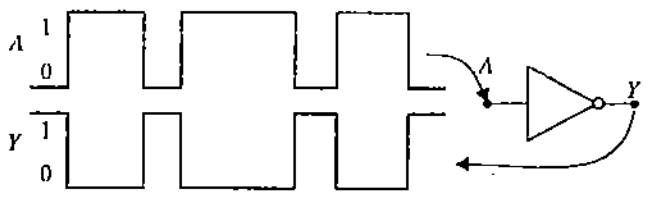


Fig. 11.14:

Solution

Recall that the output of a NOT gate is 1 if the input is 0, and the output is 0 if the input is 1. With this understanding, the output comes out to be as shown in the trace for Y in Fig. 11.14

SAQ 3

Trace the output of a NOT gate if the input is as shown in Fig. 11.15.

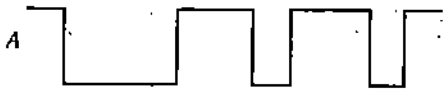


Fig. 11.15:

11.2.4 Combination of Logic Gates

The AND, OR and NOT gates are the fundamental gates for all digital circuits. These gates can be combined with each other for a particular application. However, two types of combinations are very important as you will learn now.

NAND Gate

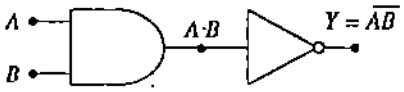


Fig. 11.16: Combination of AND and NOT gate.

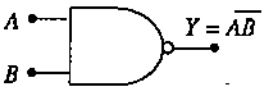


Fig. 11.17: Symbol of NAND gate.

If the output of an AND gate is given to the input of a NOT gate, as shown in Fig. 11.16, the resulting circuit is known as NAND gate the symbol for which is shown in Fig. 11.17. The truth table of this gate is obtained as follows:

A	B	Y′ (AB)	Y
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Thus the truth table of NAND gate is shown in Table 11.4.

Table 11.4: Truth table for NAND gate.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

The input-output relationship of a NAND gate is expressed as A·B = Y. The NAND gate is known as the building block for the digital circuits because using NAND gates, one can obtain AND, OR and NOT gates. This aspect will be explained later.

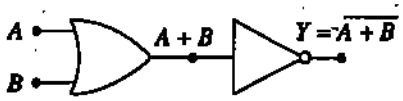


Fig. 11.18: Combination of OR and NOT gate.

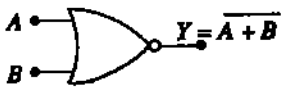


Fig. 11.19: Symbol of NOR gate.

If the output of an OR gate is given to the input of a NOT gate, as shown in Fig. 11.18, the resulting circuit is known as NOR gate the symbol for which is shown in Fig. 11.19. The truth table of this gate is obtained as follows:

A	B	Y′ (A + B)	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Thus the truth table of a NOR gate is shown in Table 11.5.

Table 11.5: Truth table for NOR gate.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

The input-output relationship of a NOR gate is expressed as $\overline{A + B} = Y$. The NOR gate is also known as the building block for the digital circuits because using NOR gates one can obtain AND, OR and NOT gates.

Example 11.4

If the inputs A and B to NAND gate are as shown in Fig. 11.20, trace the output Y.

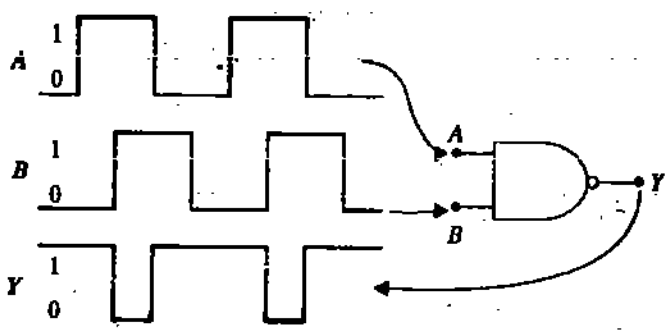


Fig. 11.20:

It is quite clear from these equations that all the four Boolean equations using AND operation satisfy the binary multiplication using bits 0 and 1. However, in the case of OR operation, while first three Boolean equation satisfy binary addition, but the last equation 1 + 1 = 1 does not. It is because in binary arithmetic 1 + 1 = 10. Despite this contradiction between Boolean and binary additions which will be settled later, the Boolean operations are very helpful in digital circuits. The Table 11.8 will lead us to various Boolean theorems which will be described in the following section.

For the moment let us see how Boolean equations are written and used for a digital circuit. Consider the circuit of Fig. 11.24 in which A and B are the inputs to AND gate

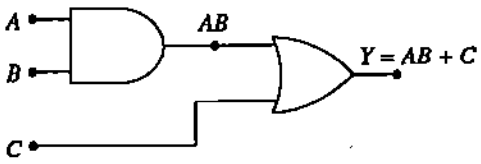


Fig. 11.24: Digital circuit for Y = A·B + C.

while C is one of the inputs to OR gate. Another input to OR gate is the output of AND gate, i.e. AB. The output of this combination is Y which is

$$Y = (A \cdot B) + C = AB + C$$

Let us find Y if, say, A = 0, B = 1, and C = 1.

$$Y = 0 \cdot 1 + 1$$

From Table 11.8, 0·1 = 0, so

$$Y = 0 + 1$$

From Table 11.8, 0 + 1 = 1. Hence,

$$Y = 1.$$

Let us now convert a given Boolean expression into a logic circuit. Say, $Y = (\bar{A} \cdot B) + (A \cdot \bar{B})$. The equation means that Y is the output of a 2-input OR gate the inputs to which are $\bar{A} \cdot B$ and $A \cdot \bar{B}$ which in turn are the outputs of two AND gates. The inputs to these AND gates are $\bar{A}$ and B and A and $\bar{B}$ respectively. The whole of this exercise is summarised in the Fig. 11.25.

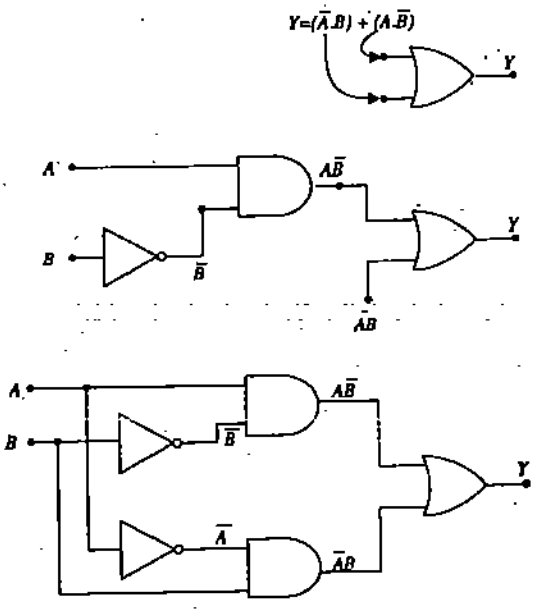


Fig. 11.25: Conversion of a boolean expression $Y = \bar{A}B + A\bar{B}$ into a digital circuit.

11.3.1 Boolean Theorems

Recalling Table 11.8 we can now write several identities or theorems which are used in Boolean algebra. It is also worthwhile to recall that

A. i) Output of an AND gate is 1 only when all the inputs are 1.

ii) Output of an AND gate is 0 when all or any of the inputs is 0.

B. i) Output of an OR gate is 0 when all the inputs are 0.

ii) Output of an OR gate is 1 when either of the inputs or all the inputs are 1.

C. Output of a NOT gate is inversion of its input.

From these conclusions and postulates, we derive the following properties or rules/law/ theorems:

From AND function,

1. $X \cdot 0 = 0$
2. $0 \cdot X = 0$
3. $X \cdot 1 = X$
4. $1 \cdot X = X$

From OR functions,

5. $X + 0 = X$
6. $0 + X = X$
7. $X + 1 = 1$
8. $1 + X = 1$

Combination variable with itself or its complement.

9. $X \cdot X = X$
10. $X \cdot \overline{X} = 0$
11. $X + X = X$
12. $X + \overline{X} = 1$

From double complementation.

13. $\overline{\overline{X}} = X$

Commutative laws for multiplication and addition. These laws show that the order in which two variables are ORed or ANDed together makes no difference.

14. $X \cdot Y = Y \cdot X$
15. $X + Y = Y + X$

Associative laws for addition and multiplication. These laws show while ORing or ANDing several variables, it makes no difference in what order the variables are grouped.

16. $X + (Y + Z) = (X + Y) + Z = X + Y + Z$
17. $X (YZ) = (XY) Z = XYZ$

Distributive laws.

18. $X \cdot (Y + Z) = (X \cdot Y) + (X \cdot Z)$
19. $X + (Y \cdot Z) = (X + Y) \cdot (X + Z)$
20. $(W + X) \cdot (Y + Z) = WY + XY + WZ + XZ$

Note here that commutative, associative and distributive laws are similar to ordinary algebra.

Absorption laws. These have no counterpart in ordinary algebra.

21. $X + X \cdot Y = X$

22. $X \cdot (X + Y) = X$

23. $X + \overline{X}Y = X + Y$

24. $X \cdot (\overline{X} + Y) = XY$

DeMorgan's theorems. First theorem says that the complement of a sum is equal to the product of complements:

25. $\overline{X + Y} = \overline{X} \cdot \overline{Y}$

Second theorem says that the complement of a product is equal to the sum of complements.

26. $\overline{X \cdot Y} = \overline{X} + \overline{Y}$

These theorems are valid even when the variables are expressions. There is no algebraic proof of these theorems. However, each theorem/law can be proved by putting the values (0 or 1) of variables and applying boolean postulates given in Table 11.8.

11.3.2 Algebraic Method for Combinational Logic

We have now know that a logic circuit can be expressed in the form of boolean expression which, in turn, can be simplified using boolean laws. We have also known that a boolean expression can also be transformed into an equivalent logic circuit.

Before we learn the simplification method and other techniques, let us understand the meaning of combinational logic. Whenever a logic circuit is explicitly defined by its truth table to provide a fixed, invariant relationship between input and output, the circuit is called the combinational circuit. A combinational circuit does not have a memory. It always operates in accordance with its truth table regardless of any prior input which may have been given to the circuit. This will be further understood after we have taken up some examples.

A boolean expression can be simplified in either of the two forms — (a) Sum of Product (SOP), and (b) Product of Sum (POS). We shall limit ourselves to only SOP form which is most commonly used. Object of simplification is to minimise the number of variables or occurrences of a variable in an expression. This means minimising operation symbols and hence the number of gates to be used in the circuit. Many a times we get more than one simplified form of an expression, each being equivalent in number of gates and variables to be used. In final analysis, we shall use the Minimum Sum of Product (MSP) form which is written without brackets. Consider the reduced expression A (B + C) which is written in MSP form AB + AC. While the reduced expression requires one AND gate and one OR gate, the MSP expression requires one AND gates and one OR gate. Thus in this case MSP expression is not the simplest. Fundamental rule is that the expression must be (a) reduced as much as possible, and (b) written without brackets. For the simplification of boolean expression, boolean operations should be carried out in the following order:

1) Inversion of single variables.

2) All operations with brackets.

3) AND operations before OR operations.

4) OR operations.

5) If an expression is with a bar, then before inverting perform all operations.

Example 11.5

1) Find the MSP expression for

$Y = (\overline{A} + \overline{B})\,\overline{C} + \overline{A}\overline{B}$

$= (\overline{A} + \overline{B})\,\overline{C} + (\overline{A} + \overline{B})$ Using DeMorgan's theorem, Th. 26

$= (\overline{A} + \overline{B})\,[\overline{C} + 1]$ Taking $(\overline{A} + \overline{B})$ common

$= (\overline{A} + \overline{B}) \cdot 1$ Using Th. 7

$= (\overline{A} + \overline{B})$ Using Th. 3

= MSP expression.

The logic circuits for the given and the MSP expressions are shown in Figs. 11.26 and 11.27 respectively.

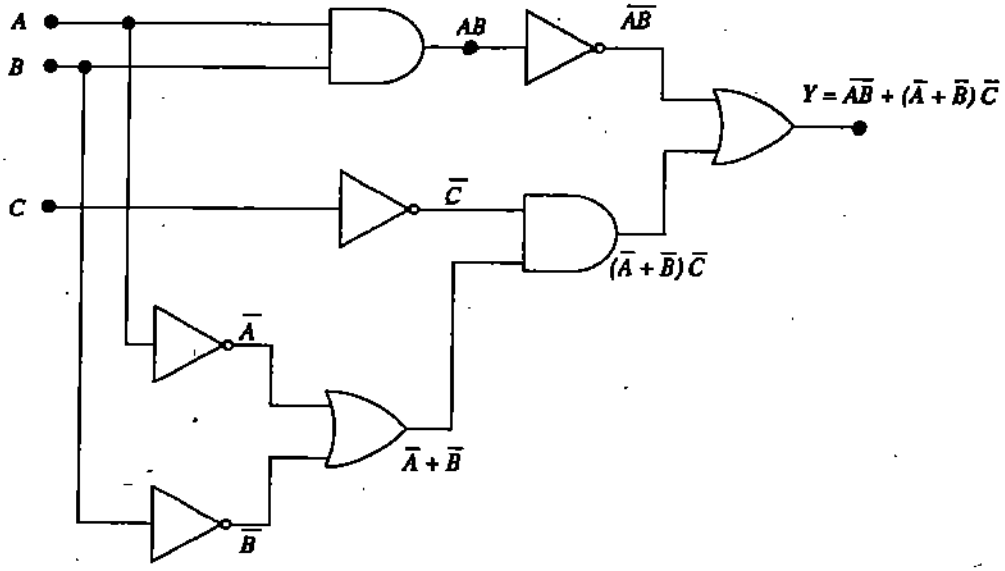


Fig. 11.26: Digital circuit for $Y = (\overline{A} + \overline{B})\,\overline{C} + \overline{A}\overline{B}$.

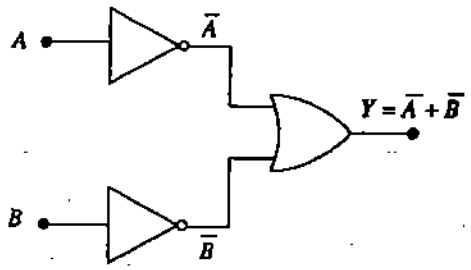


Fig. 11.27: Digital circuit for $Y = \overline{A} + \overline{B}$.

Example 11.6

Find the MSP expression for

$Y = \overline{A}C + AB\,(\overline{B} + C)$

$= \overline{A}C + AB\overline{B} + ABC$

$= \overline{A}C + A \cdot 0 + ABC$ Using Th. 10

$= \overline{A}C + ABC$ Using Th. 1

$= (\overline{A} + AB)\,C$ Taking C common

$= (\overline{A} + B)C$ Using Th. 23

$= \overline{A}C + BC$

= MSP expression

The logic circuits for the given and the MSP expressions are shown in Figs. 11.28 and 11.29 respectively.

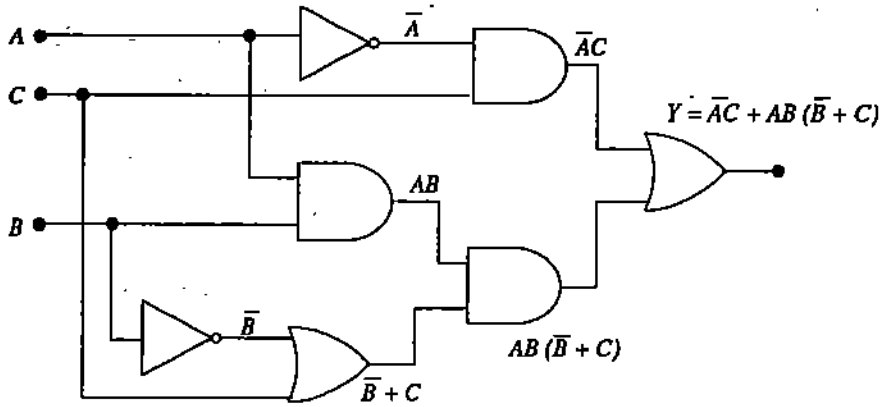


Fig. 11.28: Digital circuit for Y = $\overline{A}$C + AB ($\overline{B}$ + C).

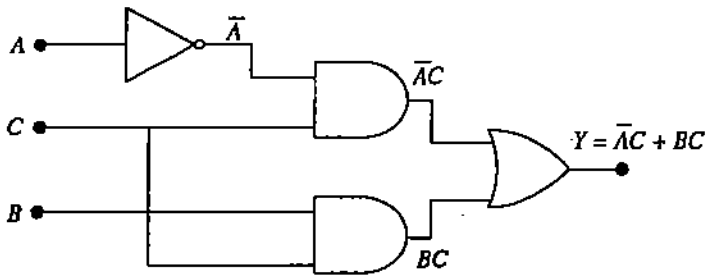


Fig. 11.29: Digital circuit for Y = $\overline{A}$C + BC.

Example 11.7

Find the MSP expression for

Y	=	AB + A (B + C) + B (B + C)	
	=	AB + AB +AC + BB + BC	
	=	AB + AB + AC + B + BC	Using Th. 9
	=	AB + AC + B + BC	Using Th. 11
	=	AB + AC + B(1 + C)	Taking B common
	=	AB + AC + B · 1	Using Th. 8
	=	AB + AC + B	Using Th. 3
	=	(A + 1) B + AC	
	=	1 · B + AC	Using Th. 7
	=	B + AC	Using Th. 4
	=	MSP expression.	

The logic circuits for the given and the MSP expressions are shown in Figs. 11.22 and 11.23 respectively.

SAQ 5

Find the MSP expression for Y = A$\overline{B}\overline{C}$ + AB$\overline{C}$ + ABC.

11.3.3 Obtaining a Truth Table from a Boolean Expression

A simplest method of obtaining the truth table from a boolean expression has already been mentioned. That is, substitute the values of variables in each possible combinations of values in the expression. Perform all the logic operations and get the result for each combination. For example,

$$Y = AB + A(B + C) + B(B + C)$$

In this expression, say, A = 1, B = 0, and C = 0, then

$$\begin{aligned} Y &= 1 \cdot 0 + 1 \cdot (0 + 0) + 0\,(0 + 0) \\ &= 0 + 1 \cdot 0 + 0 \cdot 0 \\ &= 0 + 0 + 0 \\ &= 0 \end{aligned}$$

Similarly, find Y for all combinations of values for A, B, and C, and complete the truth table which is given in Table 11.9.

Table 11.9: Truth table for Y = AB + A (B + C) + B (B + C)

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The alternative method of obtaining a truth table from a boolean expression involves reasoning. Ask yourself:

When shall the output of the expression be 1. Consider the expression

$$Y = A\overline{C} + BC = \text{MSP expression}$$

This expression is 1 so long as either $A\overline{C}$ or BC is 1. Therefore, put Y = 1 for all entries of $A\overline{C} = 1$ (i.e. entries 5 and 7). Then put Y = 1 for all entries of BC = 1 (i.e. entries 4 and 8). Now, Y for all other entries is 0. Table 11.10 is thus the truth table for the given expression.

Table 11.10: Truth table for $Y = A\overline{C} + BC$.

	A	B	C	Y
1.	0	0	0	0
2.	0	0	1	0
3.	0	1	0	0
4.	0	1	1	1
5.	1	0	0	1
6.	1	0	1	0
7.	1	1	0	1
8.	1	1	1	1

Hence, it is better to use the method of reasoning for obtaining the truth table. This method involves just two steps:

1) Obtain the MSP form of the given boolean expression, and

2) Reason out which of the truth table entries should be 1 for each product in MSP form.

Example 11.8

Obtain the truth table for the boolean expression Y = A + AB + BCD.

$$\begin{aligned} Y &= A + AB + BCD \\ &= A(1 + B) + BCD \\ &= A \cdot 1 + BCD \\ &= A + BCD \\ &= \text{MSP expression} \end{aligned}$$

Reasoning out we find that Y = 1 whenever A = 1 or the product BCD = 1. Therefore, in the truth table for this expression, put Y = 1 for all entries of A = 1, (i.e. entries 9 to 16) and put Y = 1 for all entries of product BCD = 1 (i.e. entries 8 and 16). For all other entries put Y = 0 (i.e. entries 1 to 7). The complete truth table is given in Table 11.11.

Table 11.11: Truth table for Y = A + AB + BCD.

	A	B	C	D	Y
1.	0	0	0	0	0
2.	0	0	0	1	0
3.	0	0	1	0	0
4.	0	0	1	1	0
5.	0	1	0	0	0
6.	0	1	0	1	0
7.	0	1	1	0	0
8.	0	1	1	1	1
9.	1	0	0	0	1
10.	1	0	0	1	1
11.	1	0	1	0	1
12.	1	0	1	1	1
13.	1	1	0	0	1
14.	1	1	0	1	1
15.	1	1	1	0	1
16.	1	1	1	1	1

SAQ 6

Obtain the truth table for Y = AB + BC + CA.

11.3.4 Obtaining a Boolean Expression from a Truth Table

Consider the truth table given in Table 11.12.

Table 11.12: Given truth table.

	A	B	C	Y
1.	0	0	0	0
2.	0	0	1	0
3.	0	1	0	0
4.	0	1	1	0
5.	1	0	0	1
6.	1	0	1	0
7.	1	1	0	1
8.	1	1	1	1

Note that the entries 5, 7, and 8 contribute a logic 1 to the operation while all other entries give a logic 0. To obtain the boolean expression, we need only write a product term for each entry that contribute a logic 1, and then assemble the operations by connecting all the products with a logic OR. Do as follows.

Entry 5: $Y = 1$ for $A = 1, B = 0, C = 0$

$= A\overline{B}\overline{C}$

because the output of an AND gate will be 1 only if all the inputs are 1. Similarly,

Entry 7: $Y = 1$ for $A = 1, B = 1, C = 0$

$= AB\overline{C}$

Entry 8: $Y = 1$ for $A = 1, B = 1, C = 1$

$= ABC.$

Now connect all the three products with an OR logic. Hence

$$Y = A\overline{B}\overline{C} + AB\overline{C} + ABC \text{ (Sum of Product)}$$

Which can be simplified as

$$Y = A\overline{B}\overline{C} + AB(\overline{C} + C)$$
$$= A\overline{B}\overline{C} + AB$$
$$= A(\overline{B}\overline{C} + B)$$
$$= A(B + \overline{C})$$
$$= AB + A\overline{C}$$

The procedure can be summarised as follows:

1) Combine with an AND operation all the input variables for the entries that contribute a logic 1.

2) Select for each variable in the product an overbar or no overbar so that when the input values of the entries are substituted, the product gives a logic 1. These products are also known as fundamental products.

3) The products are assembled with an OR operation.

4) The sum of product expression thus obtained may not be minimal. Use boolean algebra to bring an SP expression in an MSP form.

SAQ 7

Obtain the boolean expression for the truth table given below:

In this example of addition, the bit on the right hand side is sum while the bit on the left hand side is carry. This can be put in a truth table as shown in Table 11.15.

Table 11.15: Truth table for half adder.

A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

This application has two outputs, one for 'sum' and another for 'carry'. Therefore, we have to obtain two boolean expressions for the two outputs.

The expression for carry is

$$\text{Carry} = AB$$

that is, it is the output of an AND gate.

The expression for sum is

$$\text{Sum} = \bar{A}B + A\bar{B}$$

that is, it is the output of an XOR gate described in the previous section. These two circuits are connected together as shown in Fig. 11.34. This circuit is known as half adder and its symbol is given in Fig. 11.35.

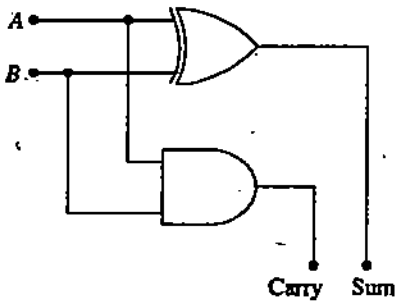


Fig. 11.34: Half adder circuit.

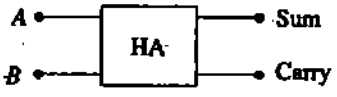


Fig. 11.35: Symbol of half adder.

Recall the contradiction pointed out while describing addition by an OR gate. While it could justify addition in case of its first three entries of inputs, it could not give correct result of addition of binary numbers in its last entry of inputs, i.e. it gave 1 + 1 = 1 (boolean addition) rather than 1 + 1 = 10 (binary addition). This contradiction is now taken care of by the design of half adder. We can now say that the binary addition should be done using half adder or circuits described later in the Unit. But as far as boolean postulates, including based on OR gate, are concerned, they are helpful in designing circuits for binary arithmetic.

11.3.8 Addition of Three One Bit Binary Numbers (Full Adder)

The full adder can add three single-bit binary numbers. The binary addition three single-bit binary numbers is as follows:

0	0	0	0	1	1	1	1
+0	+0	+1	+1	+0	+0	+1	+1
+0	+1	+0	+1	+0	+1	+0	+1
00	01	01	10	01	10	10	11

The right hand bits of these additions represent the sum and the left hand bits represent the carry. These eight possible combinations of three single-bit binary numbers can be presented in the form of a truth table given in Table 11.16.

Table 11.16: Truth table for full adder.

A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

In order to design the logic circuit for a full adder boolean expressions have to be written and simplified in MSP form for both sum and carry which are as follows:

$$\begin{aligned}
\text{Sum} &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \\
&= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC) \\
&= \bar{A}(B \oplus C) + A(\overline{B \oplus C}) \\
&= \bar{A}X + A\bar{X} \qquad \text{where } X = B \oplus C \\
&= A \oplus X \\
&= A \oplus B \oplus C \\
&= \text{MSP expression.}
\end{aligned}$$

This is the output of a 3-input XOR gate.

$$\begin{aligned}
\text{Carry} &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\
&= BC(\bar{A} + A) + A\bar{B}C + AB\bar{C} \\
&= BC + A\bar{B}C + AB\bar{C} \\
&= C(B + A\bar{B}) + AB\bar{C} \\
&= C(B + A) + AB\bar{C} \\
&= BC + AC + AB\bar{C} \\
&= BC + A(C + B\bar{C}) \\
&= BC + A(C + B) \\
&= BC + AC + AB \\
&= \text{MSP expression.}
\end{aligned}$$

From these two MSP expressions, the logic circuit for a full adder can be obtained as described earlier. This circuit is given in Fig. 11.36 and its symbol is given in Fig. 11.37.

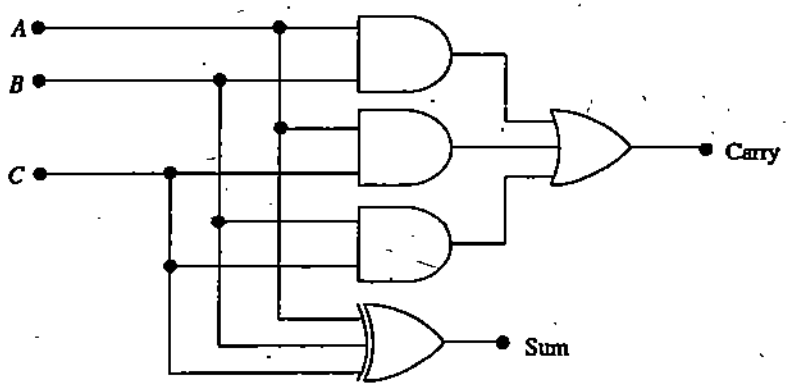


Fig. 11.36: Full adder circuit.

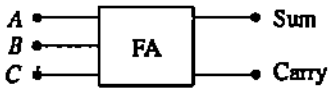


Fig. 11.37: Symbol of full adder.

You would recall that a computer or a digital circuit can add only two binary numbes at a time. If a digital circuit has to add more than two binary numbers, as would mostly be the case, the circuit will add first two binary numbers and to the sum of these two numbers it will add the third binary number, and so on. But while adding two bits a carry is likely to appear as shown above. Therefore if the two binary numbers to be added are having more than one bit, then after the addition of first bits of the numbers the addition of second bits will also require the addition of any carry which appears from the addition of first bits. Thus the addition of first bits can be carried out by the half adder which has two inputs, but the addition of second bits require a 3-input adder which is realised by the full adder. There are eight entries to the truth table of a full adder, half of which are satisfied by the truth table of half adder ignoring carry bit (because the addition of first bits of two numbers do not have a carry to be added). For this reason, the adder described in the previous section is called the half adder and the described in this section is called the full adder.

Example 11.8

Addition of two 4-bit binary numbers. Let us say the numbers are $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$. This addition requires one half adder to add A_0 and B_0 and three full adders to add rest of the bits as shown in the circuit of Fig. 11.30. The outputs of the half adder are sum (S_0) and carry. The carry output of the half adder is given as the third input to the first full adder which has a carry output and a sum (S_1) output. The carry output of the first full adder is given to the second full adder, and so on. Thus for addition of two 4-bit binary numbers, we require one half adder and three full adders. For each additional bit in the numbers to be added, we require one more full adder.

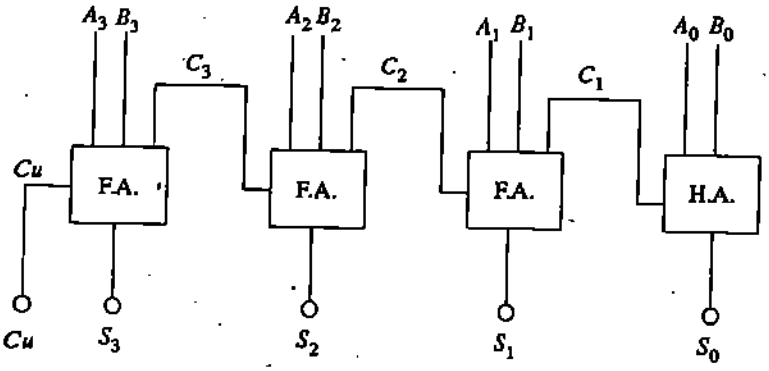


Fig. 11.38: A 4-bit binary adder.

SAQ 8

Draw a digital circuit for a 2-bit binary adder.

11.3.9 Designing Circuits Using NAND Gates Only

Quite often it is required that only NAND gates should be used in designing digital circuits. The NAND gate being universal can be used to realise AND, OR and NOT gates. Therefore, wherever these gates are appearing, the equivalent NAND circuit is used. The realisation of AND, OR and NOT gates from NAND gates is shown in Fig. 11.39.

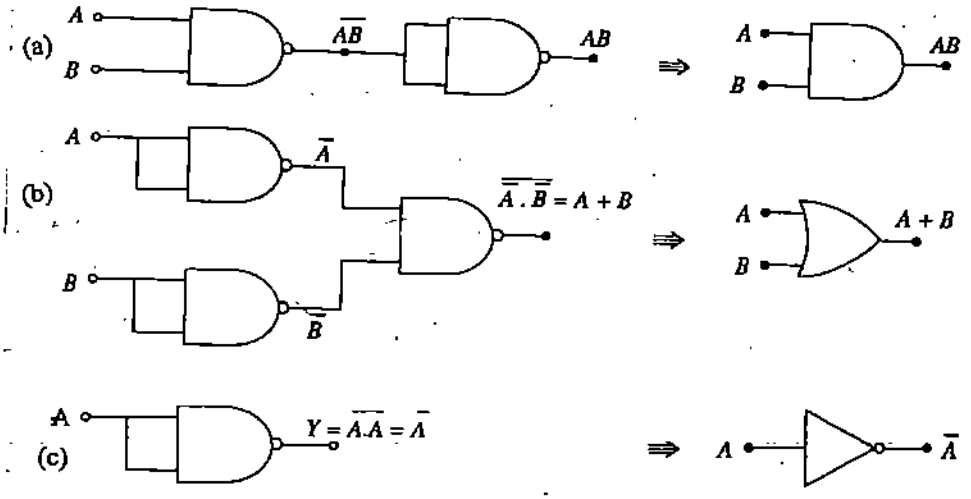


Fig. 11.39: Realisation of (a) AND, (b) OR, and (c) NOT gates using NAND gates.

Example 11.9

Design a circuit for Y = AB + CD using NAND gates only.

The circuit for Y = AB + CD using AND and OR gates is shown in Fig. 11.40.

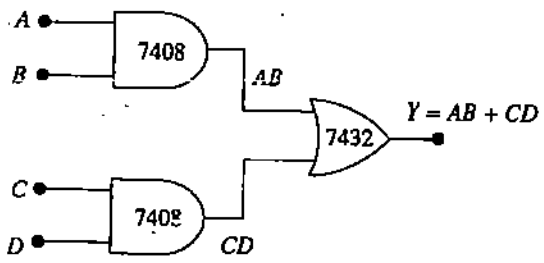


Fig. 11.40: Digital circuit for Y = AB + CD.

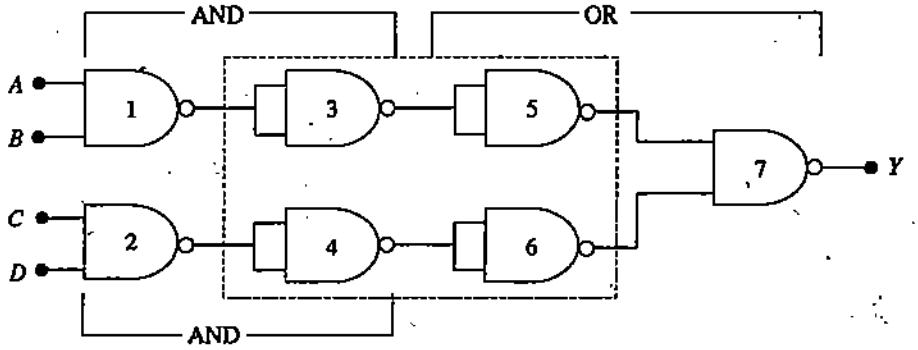


Fig. 11.41: AND and OR gates in the circuit given in Fig. 11.40 replaced by their equivalents.

The AND gates and OR gate in Fig. 11.40 are replaced by equivalent NAND gate circuits from Fig. 11.39 as shown in Fig. 11.41. It requires two NAND ICs. Since the input and output of a combination shown as dotted of a NOT gate followed by another NOT gate are same, therefore such a combination is useless and hence eliminate it. The final circuit after such elimination is shown in Fig. 11.42.

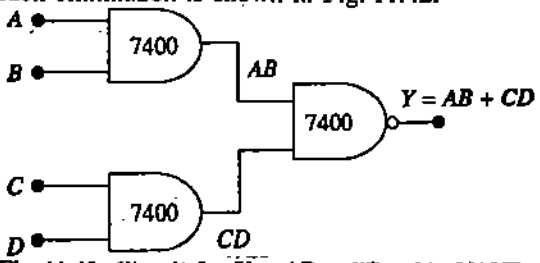


Fig. 11.42: Circuit for Y = AB + CD using NAND gates.

Another method involves the use of Demorgan's theorems. Consider the example of XOR gate. It requires one NOT IC, one AND IC and one OR IC, i.e. three ICs in total.

The MSP equation for XOR gate is $Y = \overline{A}B + A\overline{B}$. Double complement the right hand side and solve using DeMorgan's theorem.

$$\begin{aligned} Y &= \overline{\overline{A}B + A\overline{B}} \\ &= \overline{\overline{AB} \cdot \overline{A\overline{B}}} \\ &= (\overline{AB}) \cdot (\overline{A\overline{B}}) \end{aligned}$$

The right hand side is the output of a NAND gate the inputs to which are the outputs of two NAND gates, i.e. $(\overline{A}B)$ and $(A\overline{B})$. The final circuit for XOR gate using NAND gates only is shown in Fig. 11.43. It requires two NAND ICs.

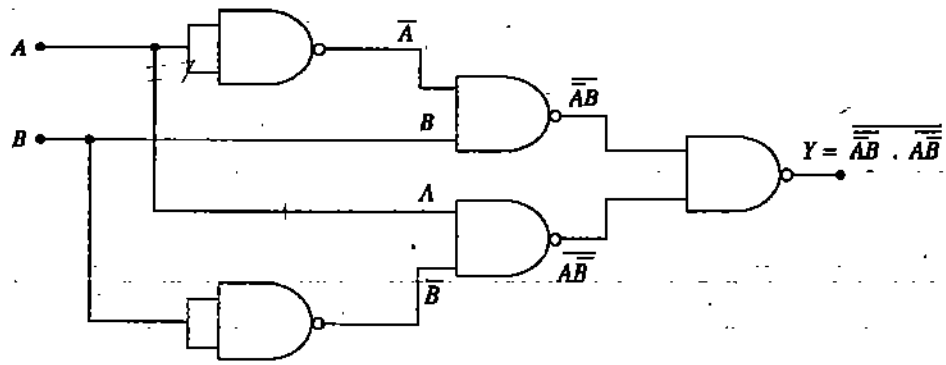


Fig. 11.43: Circuit for XOR gate using NAND gates only.

SAQ 9

Design a digital circuit for Y = A + BC using NAND gates only.

1.4 FLIPFLOPS

We have learnt combinational logic circuits in the previous section. The combinational logic circuits operate strictly in accordance with their truth table. However, there are logic circuits which have feedback path and the operation of which is not strictly defined by their truth tables. Such circuits operate differently for a given input condition depending upon the prior input sequence applied to the circuit. Such circuits are known as sequential logic circuits. These circuits have memory element also. In addition to the logic gates, a computer requires memory element. The simplest memory element is a flipflop. It has two stable states and remains in any one of these two stable states until triggered into the other state. Quite often the flipflop is also known as a latch.

11.4.1 RS Flipflop

The most basic flipflop circuit is constructed using two NAND gates or two NOR gates. In NAND gate flipflop, two NAND gates are cross-coupled as shown in Fig. 11.44. It has two latched outputs Q and $\overline{Q}$. It has two inputs: SET (S) and RESET (R) or CLEAR (C). The input names signify their actions as well. For the input names such a flipflop is known as RS flipflop.

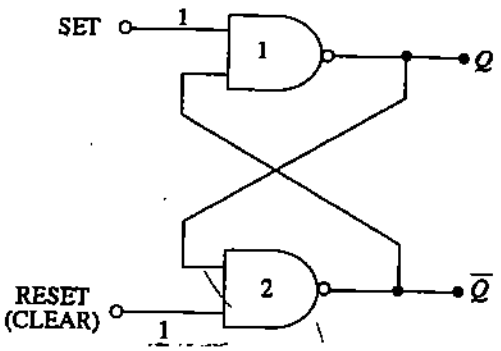


Fig. 11.44: RS flipflop.

Let us now understand the working of a RS flipflop. Both the inputs, SET and RESET, are kept HIGH, i.e. at logic 1. In the beginning, let us say S = R = 1. With the outputs Q = 0 and $\overline{Q}$ = 1, NAND-1 has the inputs 1 and 1 hence Q = 0, and NAND-2 has inputs 1 and 0, hence $\overline{Q}$ = 1. These outputs are latched or stuck with each other and continue to be latched until input conditions are changed.

Second possibility with S = R = 1 is when Q = 1 and $\overline{Q}$ = 0. The NAND-1 will have 1 and 0 inputs giving Q = 1. Likewise the NAND-2 will have 1 and 1 inputs giving $\overline{Q}$ = 0. Once again the two outputs are latched together and they will continue to be latched until input conditions are changed. S and R both high means the two sets of possible outputs remains in its last state indefinitely because of the internal latching action. Thus, a high S and a high R gives us the inactive state; the circuit stores or remembers. When we want to change the flipflop output one of the inputs will be pulsed LOW (i.e. logic 0).

Setting the Flipflop

Let us say that the SET is mometarily pulsed LOW (i.e. S = 0 for a moment) while RESET continues to be 1. Now if Q = 0 and $\overline{Q}$ = 1 prior to the occurrence of a LOW pulse at SET, Q goes 1 which in turn forces $\overline{Q}$ to a 0. Thus when SET returns to 1, the NAND-1 output remains HIGH which in turn keeps the NAND-2 output at 0.

If prior to the application of SET pulse, Q = 1 and $\overline{Q}$ = 0, then a LOW pulse at SET will not change anything because $\overline{Q}$ = 0 is already keeping the NAND-1 output to 1. Thus when SET returns to 1, the outputs are still Q = 1 and $\overline{Q}$ = 0.

Thus a LOW on the SET input will always cause the flipflop to end up in Q = 1 state. Hence, this operation is called setting the flipflop, and Q = 1 state is known as SET state.

Note the difference in symbol of clock activated by a PGT and NGT. The change in the control inputs R and S to the flipflop will not effect a change in the Q output until an active clock (CLK) transition, i.e. a PGT in case of Fig. 11.51(a) and a NGT in case of Fig. 11.51(b), occurs. The control inputs keep the flipflop ready to change and the active clock transition at the CLK input actually triggers the change. To ensure that a clocked flipflop responds properly when the active clock transition occurs, the inputs must be stable, i.e. unchanging.

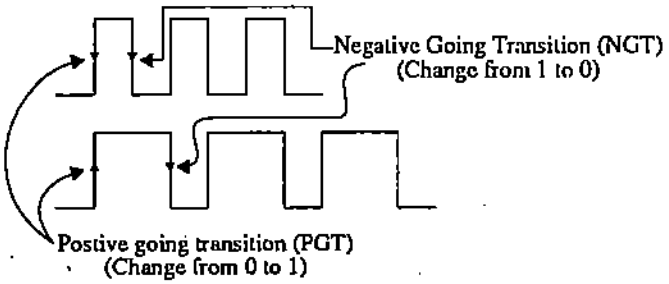


Fig. 11.50: Positive and negative going transitions.

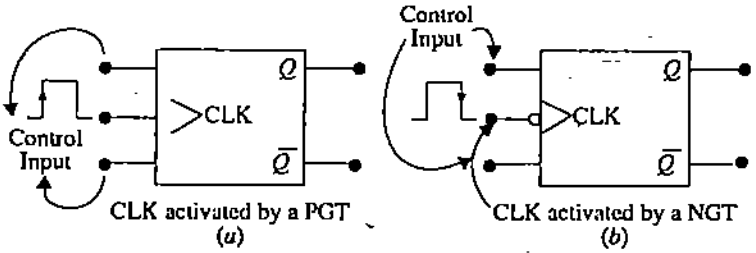


Fig. 11.51: Symbol of edge triggered flipflop activated by a (a) PGT, and (b) NGT.

Consider the circuit given in Fig. 11.52 in which two additional NAND gates are used as the clock pulse steering circuit and is triggered by a PGT. A LOW (i.e. 0) clock CLK prevents S and R from controlling the flipflop, because with whatever values of

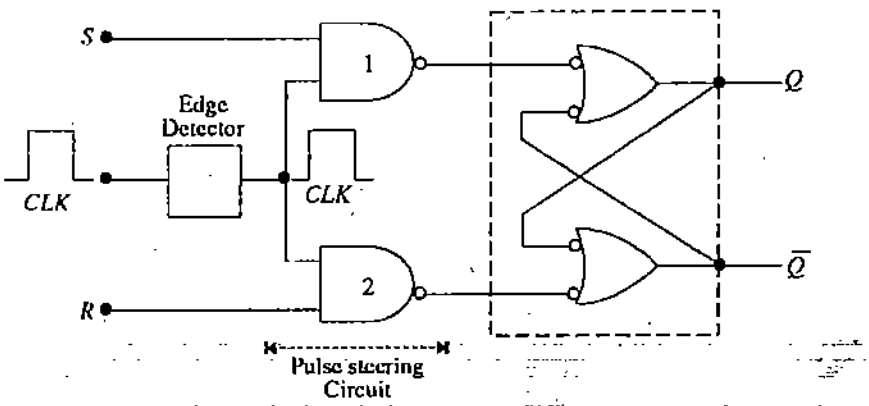


Fig. 11.52: Circuit of edge triggered RS flipflop.

S and R the outputs of the NAND-1 and NAND-2 will be 1 which will not produce any change in the Q output of the flipflop. However, when the CLK is HIGH (i.e. 1) and S = R = 0, the outputs of the two NAND gates will be 1 and there would be no change in the Q output.

Table 11.18 shows the truth table for a positive edge triggered RS flipflop. The $Q = Q_0$ is output level before the arrival of the PGT of the CLK. The arrow directed upward (↑) indicates that a PGT is required at the CLK.

Table 11.18: Truth table for a positive edge triggered RS flipflop.

Inputs			Output
R	S	CLK	Q
0	0	↑	Q_0 (No change)
0	1	↑	1
1	0	↑	0
1	1	↑	*Race

The inputs S and R, and corresponding Q output, assuming the initial value of Q, i.e. Q_0, equal to 0, are as shown in Fig. 11.53. It is clear that at the arrival of first clock transition both R and S are 0, therefore there is no change in the Q output which continues to be 0. But at the arrival of the second clock transition S is 1 and R is 0, this sets the flipflop with Q = 1 which does not change till third clock transition. At the time of the third clock transition R is 1 and S = 0 which resets the flipflop with Q = 0. This is how the Q output is traced. Note that between two PGTs of the CLK, the Q output does not change. It must be remembered that whenever tracing a Q output corresponding to the inputs, you have to look for the active clock, note the values of inputs nand then decide the value of the Q output.

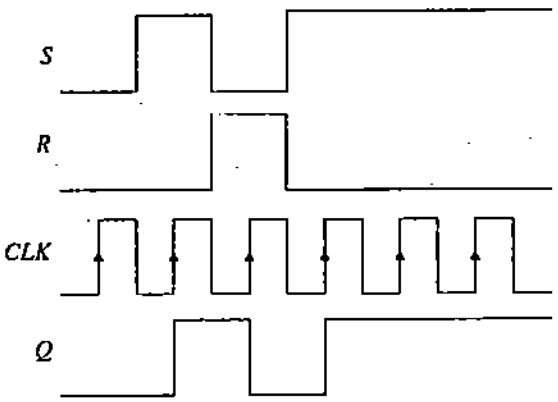


Fig. 11.53: Inputs and output of a clocked RS flipflop.

The truth table of a RS flipflop triggered by a NGT is shown in Table 11.19.

Table 11.19: Truth table for a negative edge triggered RS flipflop.

Inputs			Output
R	S	CLK	Q
0	0	↓	Q_0 (No change)
0	1	↓	1
1	0	↓	0
1	1	↓	*Race

The PGT or NGT can be obtained by using a combination of gates or a differentiating circuit consisting of a capacitor and a resistor.

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If the train of pulses to S and R inputs of a clocked RS flipflop are as shown in Fig. 11.54, and if the initial value of Q is 0, trace its Q output.

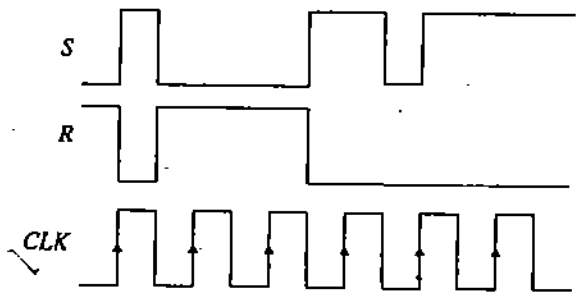

Fig. 11.54:

11.4.3 Clocked D Flipflop

The RS flipflop has two inputs S and R. Generating two signals to drive a flipflop is a disadvantage in many applications. Furthermore, the race condition of both S and R low may occur inadvertently. In order to eliminate the possibility of a race condition a new kind of flipflop is designed. This is called a D flipflop. The letter D stands for the data. The data input is given to S-input of the RS flipflop while the same input goes to its R-input through an inverter as shown in Fig. 11.55. The symbol of the edge triggered D flipflop activated by a PGT is shown in Fig. 11.56. Its truth table is given in Table 11.20 which shows that the Q output of D flipflop follows the input data D. The D input and corresponding Q output, assuming initial Q to be 1, are shown in Fig. 11.57.

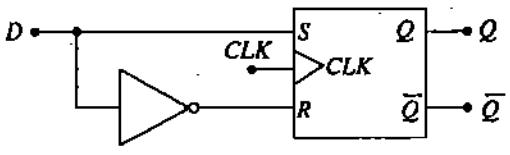

Fig. 11.55: Circuit for D flipflop.

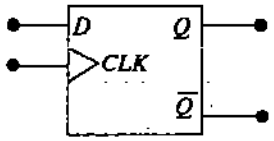

Fig. 11.56: Symbol of D flipflop.

Table 11.20: Truth table for a positive edge triggered D flipflop.

D	CLK	Q
0	↑	0
1	↑	1

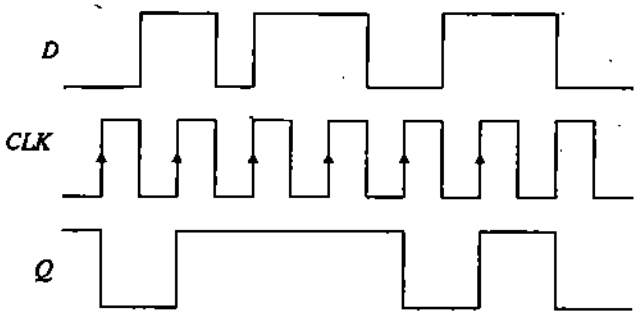

Fig. 11.57: Input and output of a D flipflop.

D Latch

Sometimes edge trigger detecting circuit (like RC combination) for D flipflop is not used. In this case the D flipflop functions slightly differently and is known as D latch. Instead of edge triggering, level clock or an ENABLE (abbreviated as EN) signal is used as shown in Fig. 11.58. When EN/CLK is 1, D will produce a 0 at either SET or CLEAR inputs of the NAND latch to give a Q output to be at the same level of D.

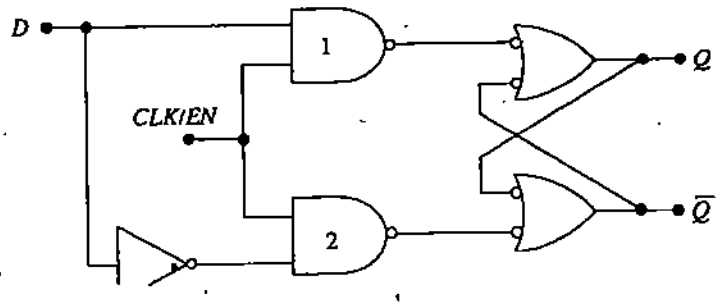

Fig.11.58: Circuit for D latch.

When EN/CLK is 1, if D changes, Q will follow changes exactly like D as the Q output does not have to wait for the clock transition to respond to changes in D. The D latch is thus 'transparent' to the input in this mode. When EN/CLK is at 0, D is inhibited from affecting NAND latch because the outputs of both steering NAND gates will be 1. Thus Q and Q continue to stay wherever they were before EN/CLK became 0. In other words, the outputs are latched to their current level and cannot change during the period EN/CLK is 0, even if D changes. The truth table of D latch is given in Table 11.21.

Table 11.21: Truth table for D latch.

D	EN/CLK	Q
X	0	NC
0	1	0
1	1	1

Quite often two AND gates are introduced between the pulse steering circuit and the NAND latch as shown in Fig. 11.59. One input each of these AND gates are known as RESET (direct SET) and CLEAR (direct RESET) and are kept at 1 so as to allow the

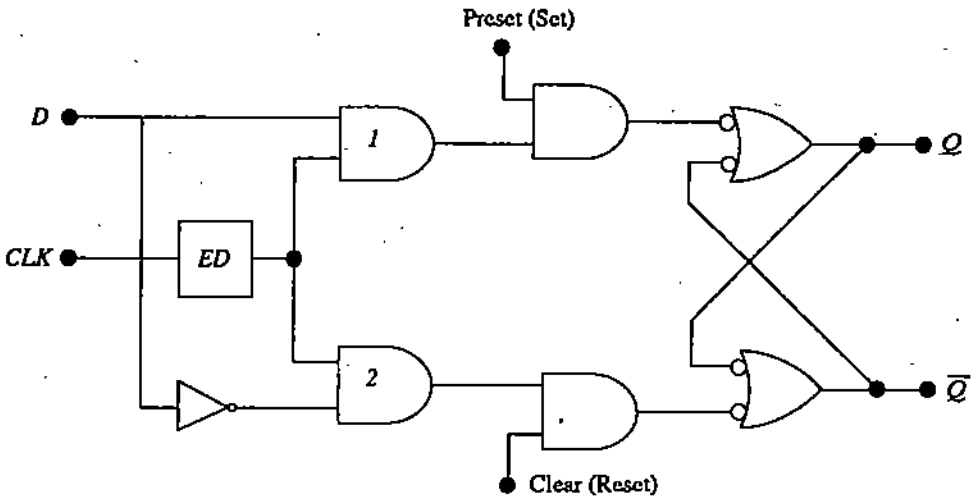

Fig. 11.59: Edge triggered D flipflop with preset and clear.

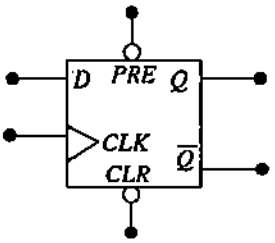

Fig. 11.60: Symbol of edge triggered D flipflop with preset and clear.

output of pulse steering circuit to pass through. However, if we want to set the flipflop irrespective of the value of D input, then give a 0 to PRESET which will set the flipflop. Similarly, by giving a 0 to clear will directly reset the flipflop. The symbol for D flipflop with PRESET and CLEAR is shown in Fig. 11.60 and its truth table is given in Table 11.22.

Table 11.22: Truth table for clocked D flipflop with preset and clear.

Preset	Clear	CLK	D	Q
0	0	X	X	*Race
0	1	X	$\tilde{X}$	1
1	0	X	X	0
1	1	0	X	NC
1	1	1	X	NC
1	1	↑	X	NC
1	1	↑	0	0
1	1	↑	1	1

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The D input to a positive edge triggered D flipflop is as shown in Fig. 11.61. Trace the Q output.

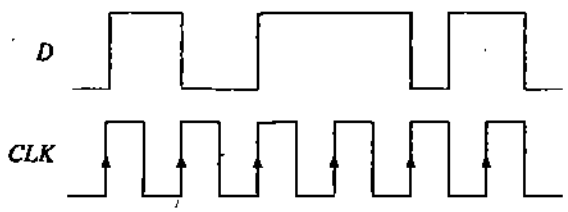


Fig. 11.61:

11.4.4 Clocked JK Flipflop

In the next unit, we show you how to build a counter, a circuit that counts the number of positive or negative clock edges driving its clock input. When it comes to circuits that count, JK flipflop is the ideal element to use. Therefore before ending this unit we will study about JK flipflop.

The circuit for an edge triggered JK flipflop is shown in Fig. 11.62 and its symbol is shown in Fig. 11.63. The working of JK flipflop is same as that of RS flipflop

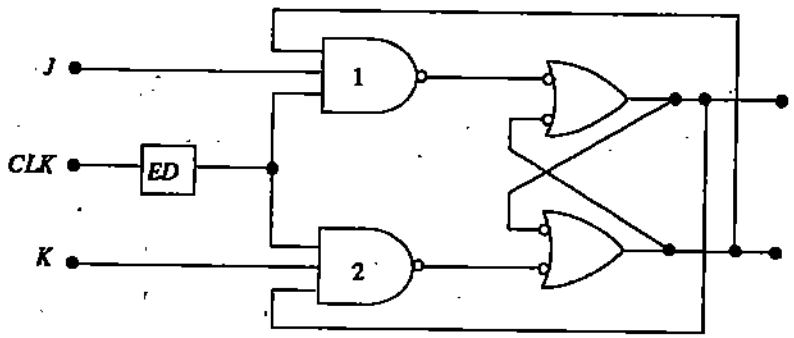


Fig. 11.62: Circuit for edge triggered JK flipflop.

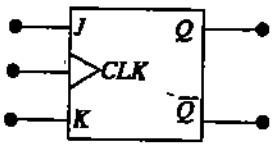


Fig. 11.63: Symbol of edge triggered JK flipflop.

except that race condition is not there. That is, there is no ambiguous result. The outputs Q and $\overline{Q}$ of the NAND latch are fedback to NAND-2 and NAND-1 respectively of the pulse steering circuit which gives toggle operation. With J = K = 1, assume that Q is 0 when clock transition arrives. With Q = 0 and $\overline{Q}$ = 1, NAND-1 will steer PGT to set the NAND latch to give Q = 1. If we assume Q = 1 when PGT of the clock appears, NAND-2 will steer PGT to clear the NAND latch to produce Q = 0. Thus Q always ends up in opposite state. This is known as the toggle mode of operation. If both J and K are left to a state of 1, the flipflop will change state for each clock transition. The Q output equal to Q_0 means that the new value of Q will be inverse of the value it had prior to the PGT. The truth table of this flipflop is given in Table 11.23. Fig. 11.64 shows J and K inputs and the corresponding Q output.

Table 11.23: Truth table for a positive edge triggered JK flipflop.

J	K	CLK	Q
0	0	↑	Q_0 (No change)
1	0	↑	1
0	1	↑	0
1	1	↑	Q_0 (Toggle)

4.

Fig. 11.70:

5. $Y = A\overline{BC} + AB\overline{C} + ABC$

$= A\overline{BC} + AB(\overline{C} + C)$

$= A\overline{B}\overline{C} + AB$

$= A(\overline{BC} + B)$

$= A(B + \overline{C})$

$= AB + A\overline{C}.$

6. Using the reasoning method, Y = 1 when either or all of AB, BC, and CA/are 1. Thus we get the truth table as follows:

Table 11.29:

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

7. $Y = \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + ABC$

8.

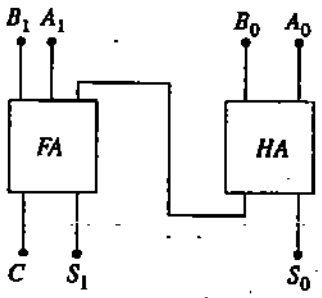


Fig. 11.71: A 2-bit binary adder.

9. Digital circuit for Y = A + BC is as shown in Fig. 11.72.

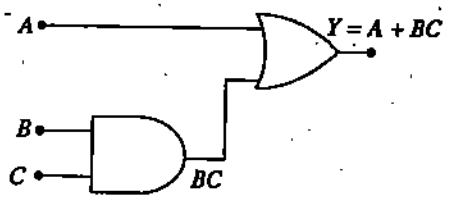


Fig. 11.72:

Now replace OR and AND gates by their NAND equivalents as shown in Fig. 11.73.

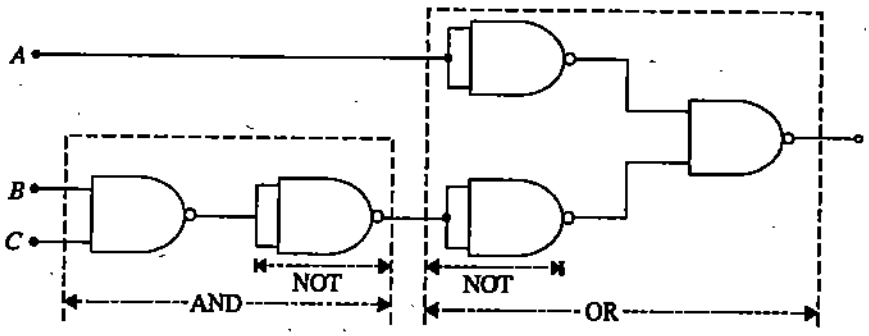


Fig. 11.73:

Removing the combination of a NOT gate followed by a NOT gate, we get the circuit as shown in Fig. 11.74.

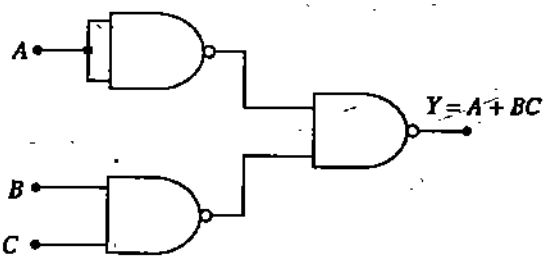


Fig. 11.74:

Alternatively, simplify the expression using DeMorgan's theorem as follows:

$$Y = \overline{\overline{A} + BC}$$

$$= \overline{\overline{A} \cdot \overline{BC}}$$

This equation gives the circuit already obtained in Fig. 11.74.

10.

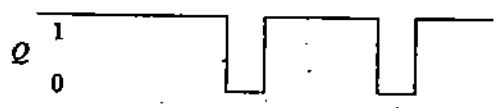


Fig. 11.75:

11.

Fig. 11.76:

12.

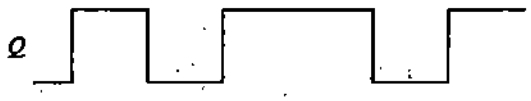


Fig. 11.77:

13.

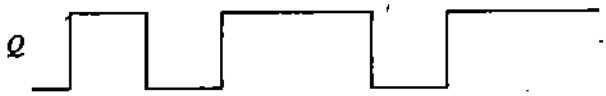


Fig. 11.78:

TQs

1. $Y = A\overline{B}D + A\overline{B}\overline{D}$
   $= A\overline{B}(D + \overline{D})$
   $= A\overline{B} \cdot 1$
   $= A\overline{B}.$

2. $Y = BCD + A\overline{B}CD$
   $= CD(B + A\overline{B})$
   $= CD(B + A)$
   $= CDB + CDA.$

3. $Y = \overline{ABCD} + \overline{ABCD}$
   $= \overline{ABD}(C + \overline{C})$
   $= \overline{ABD}.$

4. $Y = \overline{(A + BC) \cdot (D + FG)}$
   $= \overline{A} + \overline{BC} + \overline{D + FG}$
   $= \overline{A} \cdot \overline{BC} + \overline{D} \cdot \overline{FG}$
   $= \overline{A}.(\overline{B} + \overline{C}) + \overline{D} \cdot (\overline{F} + \overline{G})$
   $= \overline{AB} + \overline{AC} + \overline{DF} + \overline{DG}.$

5. $Y = \overline{ABC} + \overline{A}B\overline{C} + ABC$
   $= \overline{AC}(\overline{B} + B) + AC(\overline{B} + B)$
   $= \overline{AC} + AC.$

6. $Y = \overline{A}BC + A\overline{BC}.$

7. $Y = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}C + AB\overline{C}$
   $= \overline{A}(\overline{B}C + B\overline{C}) + A(\overline{B}C + B\overline{C})$
   $= (\overline{A} + A)(\overline{B}C + B\overline{C})$
   $= \overline{B}C + B\overline{C}.$

8. $Y = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC$
   $= \overline{AB}(\overline{C} + C) + \overline{A}B(\overline{C} + C)$
   $= \overline{A}\overline{B} + \overline{A}B$
   $= \overline{A}(\overline{B} + B)$
   $= \overline{A}.$

9.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

10.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

11.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

purpose, you have to convert the digital output in analog form. Therefore, it is necessary to have circuits which will convert an analog quantity (such as voltage) into digital form and vice versa. Such circuits are analog-to-digital (AD) and digital-to-analog (DA) converters. In this unit, you will learn different kinds of memories, and AD and DA Converters also.

Objectives

After studying this unit, you should be able to

- explain the functioning of buffer and controlled buffer registers,
- describe the functioning of the shift register,
- describe the functioning of the shift left and shift right registers,
- explain the functioning of the controlled shift register,
- explain the construction and functioning of an asynchronous (ripple) counter,
- describe the functioning of ring and mod 10 (decade) counters,
- explain several memory terms used in digital circuits,
- explain the capacity of memory and specify how many bits can be stored in a memory device,
- describe general memory operation,
- explain and distinguish between RAM and ROM,
- describe the functioning of a digital-to-analog and an analog-to-digital converters.

12.2 REGISTERS

A register is a group of memory elements which stores a binary word and it may modify the stored word in a particular fashion as is desired by the application in which it is used. It is capable of shifting the stored binary word a step or more towards left or right. In this section you will learn about them.

12.2.1 Buffer Register

The simplest kind of register is a buffer register which stores a binary word. It is made up of several D flipflops, the number of which depends on the number of bits present in a binary word. A buffer register for storing a 4-bit word, $X_3X_2X_1X_0$, with $Q_3Q_2Q_1Q_0$ as its output word is shown in Fig. 12.1.

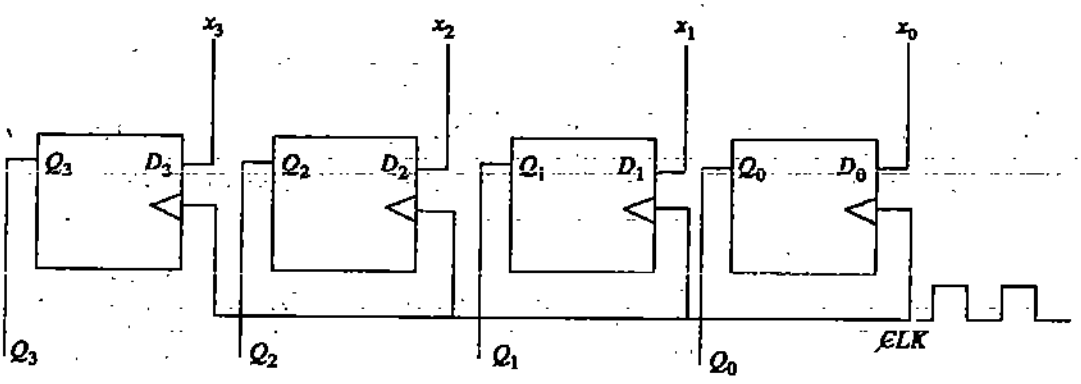


Fig. 12.1: Buffer Register.

Each flipflop is positive edge triggered. At every clock the output, Q of each flipflop is same as the input X. For this 4-bit register, we can write

$$Q_3Q_2Q_1Q_0 = X_3X_2X_1X_0$$

In chunked notation, this expression is written as

$$Q = X$$

This circuit is very basic. We should have some method to hold the input word till such time we are ready to store it. This is achieved by a controlled buffer register.

12.2.2 Controlled Buffer Register

A controlled buffer register is shown in Fig. 12.2. All flipflops are with CLEAR which resets flipflops when HIGH. The CLEAR is inactive when LOW. The control LOAD terminal when HIGH allows input X to reach the flipflop and does not allow when LOW. When CLR is HIGH, all flipflops reset and the stored word is

$$Q = 0000.$$

When CLR returns LOW, the register is ready for desired action.

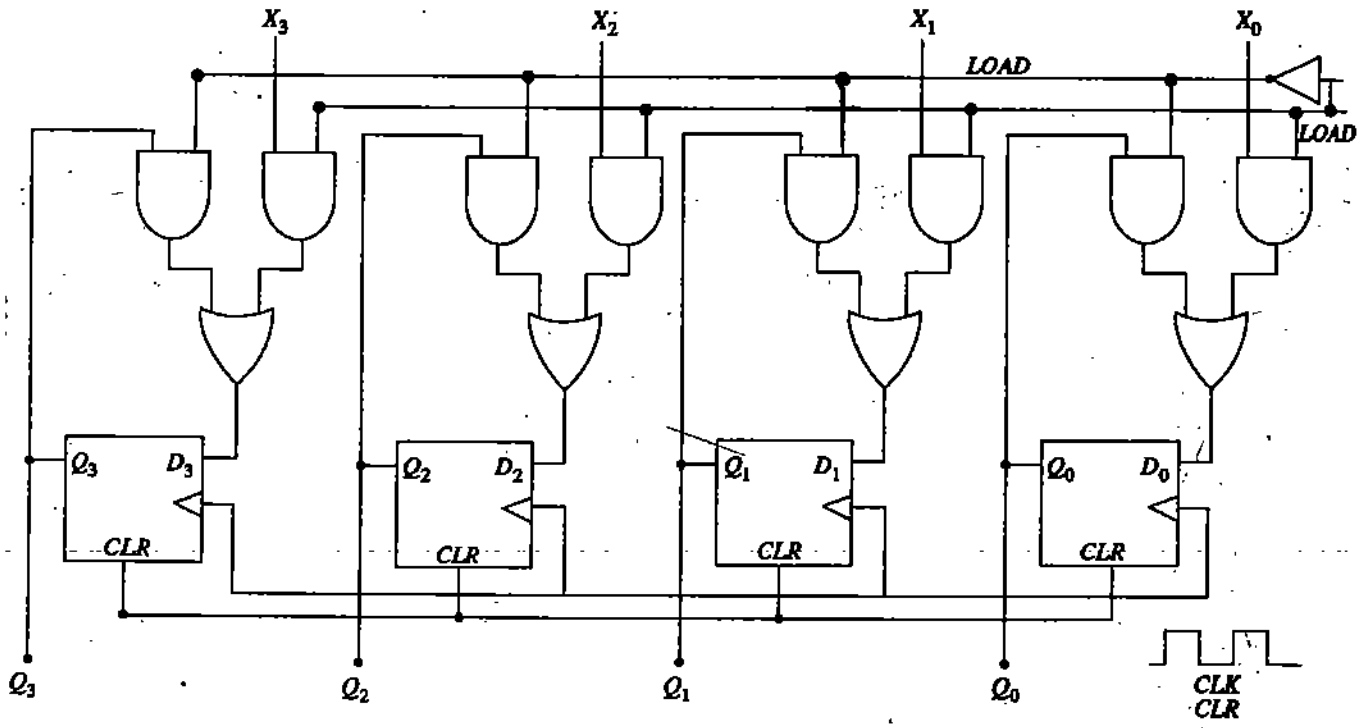


Fig. 12.2: Controlled buffer register.

The control terminal LOAD determines the circuit function. When LOAD is HIGH, the data X is allowed to reach the flipflop.

However when LOAD is LOW, $\overline{\text{LOAD}}$ is HIGH which allows the Q outputs to go to D inputs. It means that so long as the LOAD is LOW, the input data X is circulated or retained at the PGT of the each CLK. That is, the contents of the register continue to remain unchanged so long as LOAD is LOW.

When the LOAD is made HIGH, the word or data X is transmitted to the D inputs and the flipflops are ready to change. When the PGT of the CLK arrives, the X input is loaded and is available at Q outputs, and

$$Q_3Q_2Q_1Q_0 = X_3X_2X_1X_0$$

With LOAD returning to LOW, the input word is stored. That is, so long as the LOAD remains LOW, it is not affected even when X input is changed. In this kind of register, as is seen from the circuit, the input is given to all the flipflops simultaneously and the output is also obtained from all the flipflops simultaneously. This is quite often referred to as parallel-in/parallel-out register.

12.2.3 Shift Registers

The shift registers move the stored word towards left or right. Therefore there are two types of shift registers — Shift-left and shift-right registers. Shifting of bits of the stored word towards left or right is essential in arithmetical operations.

Shift Left Register

A register which shifts the bits of the stored word towards left, called shift-left register, is shown in Fig. 12.3. As is clear from the circuit, the data input D_{in} sets up first flipflop, and the Q_0 output of this flipflop sets up second flipflop, Q_1 sets up the third and Q_2 sets up the fourth. Since the data is given to the input of the first flipflop, i.e., D_{in} and the output is obtained simultaneously from all the flipflops, the circuit is known as serial-in/parallel-out.

The working of shift-left register can be understood by the following example:

Consider that the input data D_{in} is 1, i.e., the input to flipflop-1, $D_0 = 1$ and the initial output

$$Q = 0000.$$

That is, initially the inputs to all the other three flipflops are 0. Now with the arrival of the PGT of the first CLK, the Q_0 output is 1, and the stored word becomes

$$Q = 0001.$$

Now with $D_1 = 1$ and $D_0 = 1$, when the PGT of the second CLK arrives then first and second flipflops are set making the register output to be

$$Q = 0011.$$

Now $D_2 = 1$, $D_1 = 1$, and $D_0 = 1$. When the PGT of the third CLK arrives then first, second and third flipflops are set making the register output to be

$$Q = 0111.$$

Similarly when the PGT of the fourth CLK arrives, then output becomes

$$Q = 1111.$$

The stored word is thus 1111 and it remains unchanged so long as $D_{in} = 1$. However, if $D_{in} = 0$, then with successive CLK pulses the register output or content becomes

At 1st CLK $Q = 1110$

At 2nd CLK $Q = 1100$

At 3rd CLK $Q = 1000$

AT 4th CLK $Q = 0000$

This word 0000 remains stored so long as $D_{in} = 0$. The entire operation of the shift-left register in terms of its timing diagram is shown in Fig. 12.4.

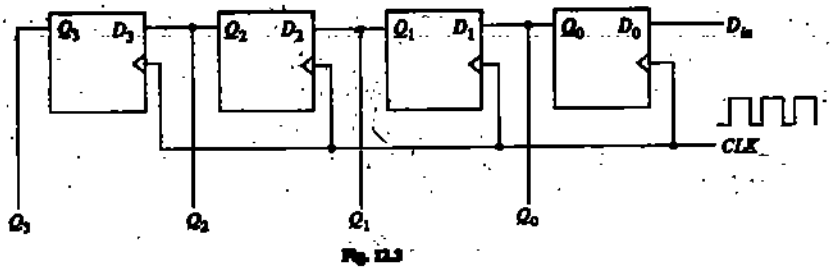


Fig. 12.3

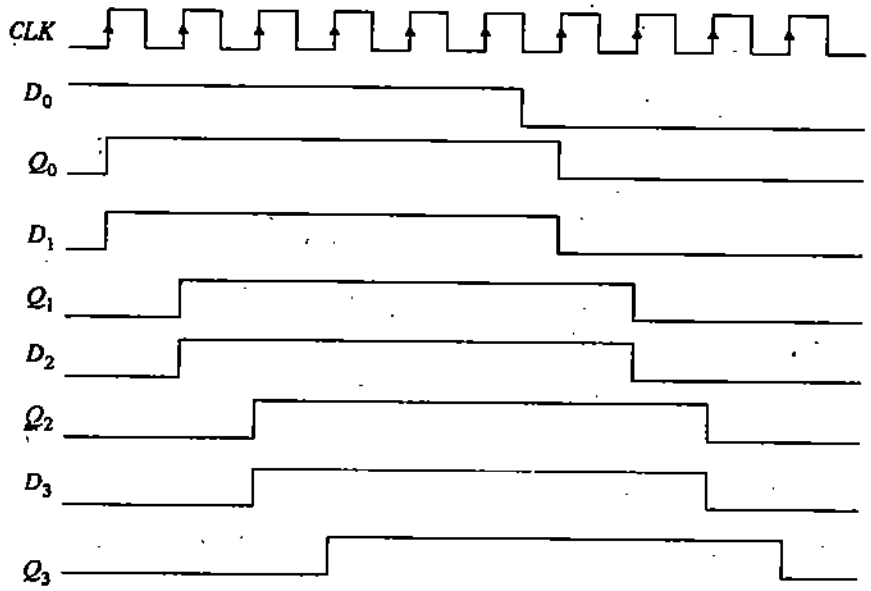


Fig. 12.4: Timing diagram of shift-left register.

Shift Right Register

The circuit for a shift-right register is shown in Fig. 12.5. The data input, D_{in} is given to the input of the fourth flipflop as D_3. The Q output of each flipflop is fedback to the D input of the previous flipflop, i.e. Q_3 is given to D_2, Q_2 is given to D_1, and Q_1 is given to D_0. When the PGT of the CLK arrives, the stored word shifts one step to its right.

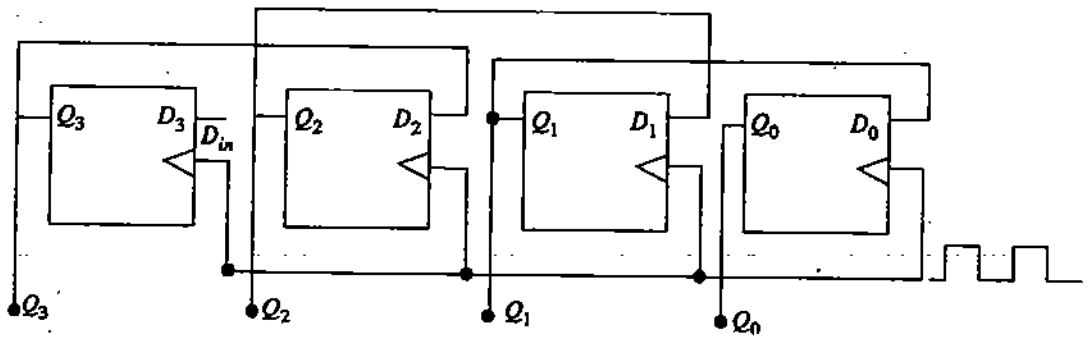


Fig. 12.5: Shift-right register.

The operation of the shift-right register can be understood as follows. Consider that in the beginning D_{in} = 1, and

Q = 0000.

At the arrival of the PGT of the first CLK, D_3 = 1, and all other D inputs are 0. Therefore, the fourth flipflop is set and the stored word is

Q = 1000.

Now D_3 = 1 and D_2 = 1. When the PGT of the second CLK arrives, third and fourth flipflops are set, and the stored word becomes

Q = 1100.

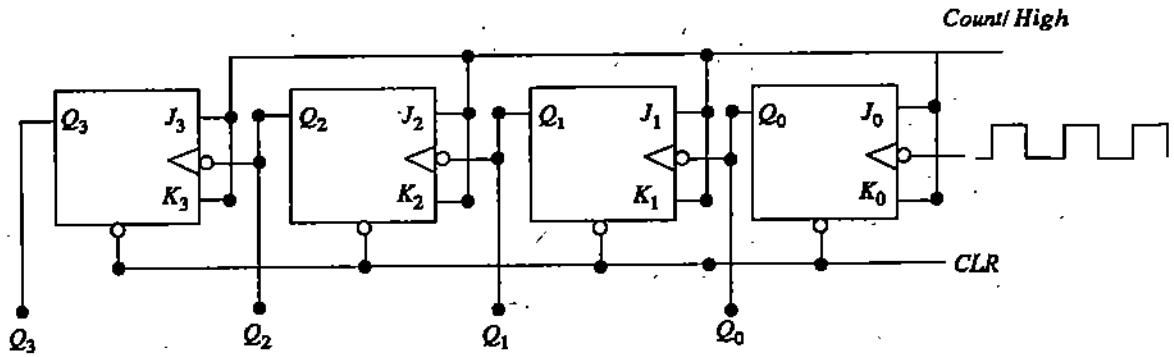


Fig. 12.8: Asynchronous (ripple) counter.

Let us understand the operation of the ripple counter. The clock pulses are applied to the CLK input of the first flipflop. Since the flipflops are driven by the NGT of the CLK, with J = K = 1, the first flipflop toggles when the CLK pulse goes form 1 to 0. The Q_1 output of second flipflop toggles when Q_0 output of the first flipflop goes from 1 to 0, and so on. With CLR = 0, all the flipflops are reset to

Q = 0000.

After resetting keep CLR = 1. Now the counter is ready to count. The Q_0 toggles for each NGT. Therefore, when the NGT of the first CLK arrives, then the Q output is

Q = 0001.

At the second CLK, Q_0 toggles from 1 to 0 which acts as a NGT for the CLK input of the second flipflop, the Q_1 output of which toggles to 1. Therefore,

Q = 0010.

At the third CLK, Q_0 toggles from 0 to 1, and there is no change in Q_1. Therefore,

Q = 0011.

At the fourth CLK, Q_0 toggles from 1 to 0 resulting in toggling of Q_1 from 1 to 0. The Q_1 going from 1 to 0 acts as a NGT for the CLK input of the third flipflop, the Q_2 output of which toggles from 0 to 1. Therefore,

Q = 0100.

The Q output of the counter at each CLK is summarised in Table 12.1.

Table 12.1:

No. of CLK pulses	Q
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

Next CLK resets all the flipflops and the Q outputs on successive CLK would be

16	0000 (recycles)
17	0001
18	0010
..	....
..	....

While analysing the Q outputs, we find that whenever a flipflop resets to 0, the output of the next flipflop is 1. That is, resetting of a flipflop send a carry to the next higher flipflop. Therefore, the counter acts like a binary odometer. The Q_0 output of the first flipflop acts as a LSB and that of the last flipflop as the MSB. This would now be clear as to why asynchronous counter is called a ripple counter. It is because the carry in the output moves like a ripple on water.

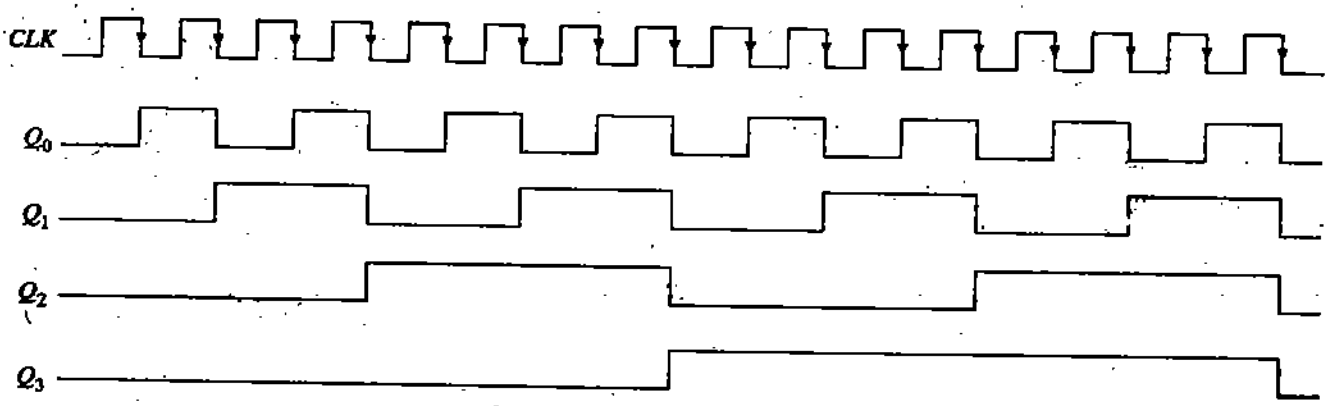
Mod of a Counter

The counter described above has 16 distinct states or outputs (0000 to 1111). It is said that the Mod number of this counter is 16. The Mod number of a counter is equal to the number of states which the counter goes through in each complete cycle before it recycles back to its starting state. The Mod number can be increased by increasing the number of flipflops. If n is the number of flipflops used in a counter, then

$$\text{Mod Number} = 2^n.$$

Frequency Division

The output of each flipflop and the CLK are shown in Fig. 12.9. It is clear that the frequency of Q_0 output is half the frequency of the CLK. The Q_0 output acts as a CLK to the second flipflop, and the frequency of its Q_1 output is half the frequency of Q_0 or one-fourth the frequency of the CLK.



First flipflop divides by	2
Second flipflop divides by	4
Third flipflop divides by	8
Fourth flipflop divides by	16
nth flipflop divides by	2^n.

expected output at the arrival of 5th CLK is 101 which should be used to activate CLR to reset the flipflops. The required circuit is given in Fig. 12.14.

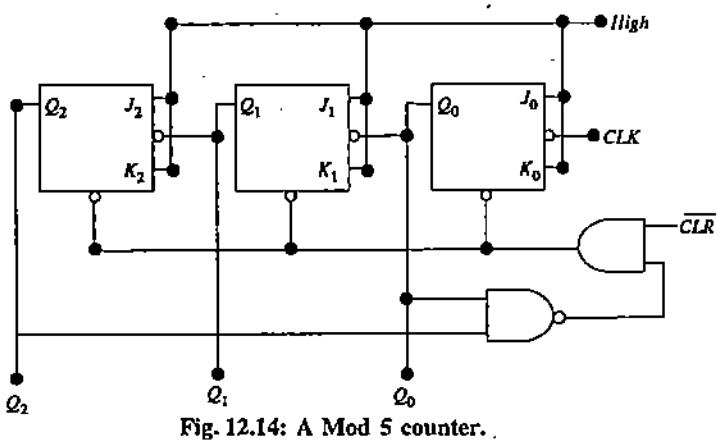


Fig. 12.14: A Mod 5 counter.

SAQ 2

What is the Mod of a counter which consists of six flipflops?

12.4 SEMICONDUCTOR MEMORIES

The advantage of digital systems over analog systems is their ability to store information for short as well as long periods which makes them versatile. A digital computer has a minimum amount of memory with the help of which it is able to manipulate information or data as desired by us. It also has memory which makes it capable of storing this information as long as we want and make it available to us whenever we want.

We have already studied about the basic memory element which stores a single bit, that is the flipflop. We have also learnt about registers which store a word of any number of bits. The registers are very high speed memory elements and are used extensively in the internal operation of a digital computer. With the invent of integrated circuit technology and its further advancement in LSI (Large Scale Integration) and VLSI (Very Large Scale Integration), a large number of registers can be obtained on a single chip.

The cost of these semiconductor devices is also decreasing. However, the cost of these devices per bit of storage is very high which prohibits their use as mass storage devices. A computer has internal memory which is constantly in communication with the central processing unit of the computer as a program of instructions is being executed. The program and any other information or data used by the program are also stored in the internal memory.

The mass storage memory devices are external to the computer and are capable of storing millions of bits even without requiring any electrical power. The mass storage memory is generally very slow compared to the internal memory and the information stored is the one which is not currently required by the computer. It is supplied to the computer only when required. The mass storage memory devices are floppies, magnetic tapes and disks, etc. The cost of per bit storage of these device is much less compared to the internal memory.

12.4.1 What a Memory is!

A 'memory' is simply an array of registers, and each register storing a word. Every register has an address number which identifies the location of a word in a memory. The location of a word is nothing but the register that stores the word to be identified. The address of each location is unique and is described by a binary number. To illustrate, let us consider that we have a memory which consists of eight registers. It is clear that this memory has eight memory locations. The unique addresses of the memory locations are given in Table 12.4.

Table 12.4:

Address	Location
000	word 0
001	word 1
010	word 2
011	word 3
100	word 4
101	word 5
110	word 6
111	word 7

Each word in the memory is thus identified by an address. By a read operation, the binary word stored in a memory location is sensed and, if desired, it can be transferred to another device. For example, if we have to read word 6, then we have to do read operation on address 110. By a write operation, a new word can be placed or stored on a particular memory location.

The memories are volatile and nonvolatile. A memory is volatile if it requires electrical power to store information and if the power is removed then the stored information is lost. Many types of semiconductor memories are volatile. The nonvolatile memory retains the stored information even when electrical power is removed. The mass storage memory devices fall in this category. The other types of memories like Random-Access Memory (RAM) and Read Only Memory (ROM) will be described in later sections.

12.4.2 Capacity of Memory

Before understanding the meaning of capacity of memory let us know some of the memory terms. A device, such as a flipflop, which can store a single bit (0 or 1) is called a memory cell. In a memory a group of bits or cells which represents instructions or data is known as a memory word. A register consisting of four flipflops is a memory which can store a 4-bit word. Similarly, a register having eight flipflops is a memory which can store a 8-bit word. The size of the word in modern computers range from 4 to 64 bits. A 4-bit word is called a nybble and 8-bit word is called a byte. A byte is the most commonly used word size.

The capacity of a memory is a term used to express how many bits can be stored in a particular memory device or in a complete memory system. For example, let us say that we have a memory which can store 2048 eight-bit words. This memory can store $2048 \times 8 = 16384$ bits and we say that this memory can store 16384 bits. Another way to express this capacity is as 2048×8. This kind of expression of memory means that there are 2048 words and the size of the word is 8 bits. The number of words in a memory is generally a multiple of 1024. The figure of $1024 = 2^{10}$ is commonly represented as '1K'. Thus memory capacity of 2048×8 is also expressed as $2K \times 8$. For larger memories, '1M' or '1 meg' is used for $2^{20} = 1,048,576$. Therefore, a $4M \times 8$ memory has a capacity of $4,194,304 \times 8$ or alternatively of 33,554,432 bits.

Example 12.2

A user has two memory devices. One of these stores 10M words of 8-bit size, while the other stores 2M words of 16-bit size. Which of the two stores most bits?

Solution

The two memories are of $10M \times 8$ and $2M \times 16$.

$10M \times 8 = 10 \times 1,048,576 \times 8 = 83,886,080$ bits.

$2M \times 16 = 2 \times 1,048,576 \times 16 = 33,554,432$ bits.

Therefore, the memory of $10M \times 8$ stores more bits.

12.5 A/D AND D/A CONVERTERS

As pointed out in the introduction of this unit, digital systems or computers perform all of their functions and internal operations using digital circuits which require digital inputs. A digital quantity will have a value either 0 or 1, while an analog quantity can take any value over a continuous range of values and its exact value is significant. Most physical variables are analog in nature, such as temperature, pressure, light intensity, audio signals, position, speed, etc. Therefore, it is essential to put an analog quantity to be analysed using a digital system first in a digital form. The analog-to-digital (A/D or ADC) converter is a digital circuit which converts an analog quantity into digital form consisting of a number of bits that represents the value of the analog input. This circuit is used as an interface between the digital system or computer and the analog system of the input stage. The output of a digital system is digital and has to be converted back into analog quantity. The digital-to-analog (D/A or DAC) converter serves this purpose and its output is a proportional analog voltage or current corresponding to an analog quantity. This is used as an interface between the digital system or computer and the analog system of the output stage.

Pictorially this is summarised in Fig. 12.18. Let us say that in a physical system a quantity, such as temperature, is to be controlled using a computer. This physical quantity is first converted into a corresponding voltage or current with the use of a transducer. A transducer is a device which converts a physical variable into an electrical signal. Thermistors, bolometers, photocells, thermo-couples are some of the commonly available transducers. Actuator used in this illustration is a device that controls the physical quantity, temperature, in a computer controlled system. In this section, we shall learn about design and working of digital-to-analog and analog-to-digital converters.

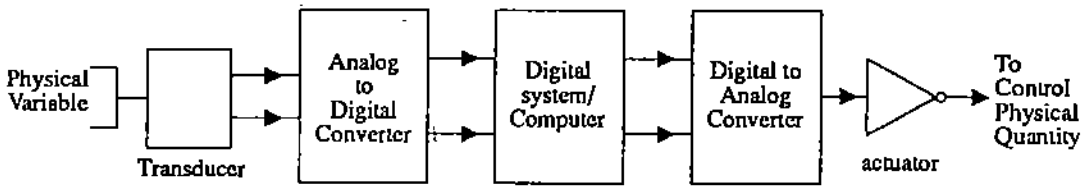


Fig. 12.18: ADC and DAC used as interfaces.

12.5.1 Digital-to-Analog Converter

We are first treating Digital-to-Analog Converter (DAC) because the Analog-to-Digital Converter (ADC) requires the use of DAC. The circuit for DAC takes the BCD or binary input and converts it to a voltage or current that is proportional to the digital value. The digital input is generally derived from an output register of the digital system which can theoretically be of any number of bits. In general, the registers used are 8-bit registers. For the purpose of an illustration, let us consider that the digital output from the digital system is of four bits. Therefore, we require a DAC that can convert a 4-bit digital output to a proportional analog value.

A block diagram of such a DAC is shown in Fig. 12.19. It has four binary input lines representing $A_3A_2A_1A_0$ and one output line representing corresponding proportional analog quantity. Each 4-bit input has unique proportional output voltage. There are 2^4 = 16 states that the binary input can have. Let us say that each input specifies a decimal number. Let us designate 1V output equivalent to decimal number 1, 2V as number 2, and so on.

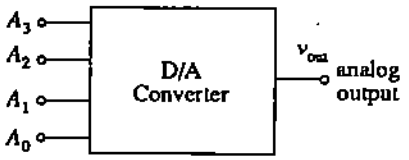


Fig. 12.19: Block diagram of DAC.

The digital input and the corresponding proportional voltage as the analog output is summarised in Table 12.5 In this example, the analog output voltage is equal in volts to the binary number. The out put voltage could be twice the binary number or any multiple. We can, therefore, write

Analog output = k × digital input

Where k is proportionality factor, a constant for a (12.1) given DAC.

The value of k in the given example is 1V, therefore V_{out} is 1V times the digital input. For $0110_2 = 6_{10}$, we get

$$V_{out} = 1V \times 6 = 6V.$$

Table 12.5:

A_3	A_2	A_1	A_0	V_{out}
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Analog Output

The DAC output is technically not an analog quantity. It can have only specific values. In the above example, it can have values only from 0 to 15 in steps of 1, that is 1, 2, 3, ..., 15. Therefore, strictly speaking it is digital. By increasing the number of input bits, the number of possible output values can be increased and the difference between successive values decreased. Thus the output can be made more or less analog. For the time being we can only say that the DAC output is pseudo analog.

DAC circuit

There are several methods and circuits for digital to analog conversion which need not be known. A basic DAC circuit is obtained using an op-amp as a summing amplifier. A 4-bit DAC circuit is shown in Fig. 12.21. The input resistors are binary weighted, that is they are in the ratio of 1 : 2 : 4 : 8. The output voltage of this circuit is given as

$$V_{out} = -(V_{A3} + \frac{1}{2} \cdot V_{A2} + \frac{4}{4} \cdot V_{A1} + \frac{1}{8} \cdot V_{A0})$$

Negative sign indicates that it is an inverting amplifier. Note that the digital input bits can be either 0 or 1, therefore V_{A3}, V_{A2}, V_{A1}, V_{A0} will have values either 0 or 5V.

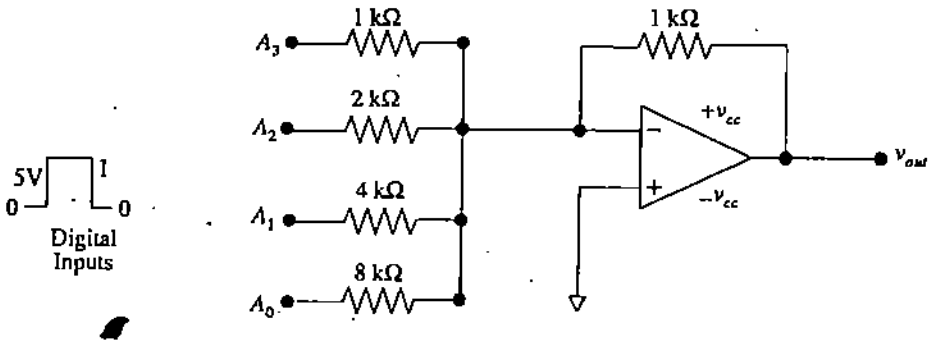


Fig. 12.21: A 4-bit DAC.

Therefore, V_{out} for 0001 or LSB would be one-eighth of 5V, i.e. 0.625V. And this is the step size of this converter. Sixteen levels of the V_{out} are shown in Table 12.7.

Table 12.7: Ideal values of V_{out} for a 4-bit DAC.

A_3	A_2	A_1	A_0	V_{out}
0	0	0	0	0
0	0	0	1	−0.625 LSB
0	0	1	0	−1.250
0	0	1	1	−1.875
0	1	0	0	−2.500
0	1	0	1	−3.125
0	1	1	0	−3.750
0	1	1	1	−4.375
1	0	0	0	−5.000
1	0	0	1	−5.625
1	0	1	0	−6.250
1	0	1	1	−6.875
1	1	0	0	−7.500
1	1	0	1	−8.125
1	1	1	0	−8.750
1	1	1	1	−9.375 MSB Full Scale

These values are ideal values. However, the actual values may not be same. There may be some error due to fluctuations in the voltages or inaccurate resistors. The error in a DAC is specified by a term called full scale error which is the maximum deviation of the DAC's output from its expected ideal value expressed as the percentage of the full scale (FS). Let us say that a DAC has an error of + 0.01 % FS in the example considered above. It means that error is 0.01 % of 9.375V, i.e + 0.9375 mV.

SAQ 6

What are the weights of each input bit of Fig. 12.21.

Example 12.6

If in the DAC circuit of Fig. 12.21, R_F is reduced to half , i.e. 500Ω, then what will V_{out} be for 1001?

Solution

The MSB passes with gain 0.5. Therefore, its weight is reduced to half of the previous case. That is, it is now 2.5V. Thus each input weight is the half of the previous case, i.e. 1.25, 0.625 and 0.312V. The V_{out} for 1001 is

$$2.5 + 0 + 0 + 0.312 = 2.812V.$$

12.5.2 Analog-to-Digital Converter

The circuit of a counter type (or digital ramp) Analog-to-Digital Converter (ADC) is shown in Fig. 12.22. It consists of an op amp as a comparator, a DAC, counter and a 3-input AND gate. The functioning of this type of ADC is as follows:

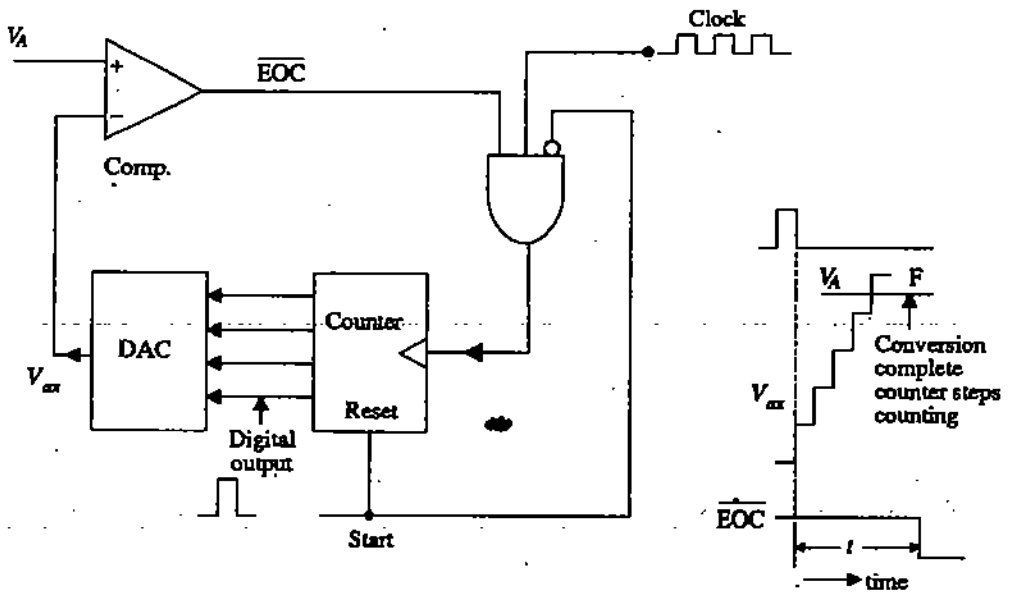


Fig. 12.22: Counter type ADC.

Apply start pulse, i.e. make START input equal to 1. This resets the counter to 0 output. With 1 at START input, the AND gate is inhibited which does not allow the CLK from passing through the AND gate. The counter output is the input to the DAC. With counter reset, the DAC output $V_{ax} = 0$. V_A is the analog input to be converted into its digital equivalent. Since $V_{ax} < V_A$, the op amp comparator output EOC is HIGH, i.e. 1. When the start pulse returns to 0, AND gate allows the CLK to pass through and the CLK reaches the counter which starts counting. As the counter advances, the DAC output V_{ax} advances step by step as shown in the figure. When V_{ax} reaches a step that

2) The word size of the computer X is 8 bits and that of computer Y is 16 bits.

For computer X

$1M \times 8 = 1 \times 1{,}048{,}576 \times 8 = 8{,}388{,}608$ bits

For computer Y

$500 \times 1024 \times 16 = 8{,}192{,}000$ bits.

Therefore, computer X can store more bits.

3) Follow Example 12.4. Smallest change in the output voltage is 0.5V. The output voltage for 1001 is 4.5V.

4) $00110010_2 = 50_{10}$

$1\ V = K \times 50$

Therefore, $K = 20$ mV.

The largest output will occur for $11111111_2 = 255_{10}$.

$V_{out(max)} = 20\ mV \times 255$

$= 5.10V.$

5) Follow the example 12.6. The resolution is 0.312V and the output voltage for 1101 is 4.062V.

UNIT 13 ELECTRONIC INSTRUMENTS

Structure

13.1 INTRODUCTION

As you are aware, in practical applications of a system, we typically encounter a situation as shown in Fig. 13.1. In study of Signal Processing Circuits we assume that we have the

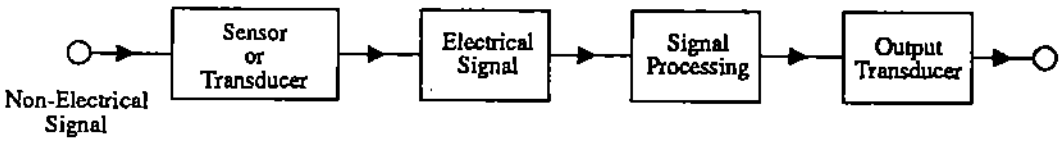


Fig.13.1: Situation encountered in practical applications of a system.

desired electrical signal and do not worry about input sensor. The performance of a circuit is displayed on an instrument which can be seen by us. The signals of different shapes and time duration are provided by signal generators and a general purpose oscilloscope is used to display them.

We know that all circuits are made up of some active components like transistors, FET, MOSFET etc. and passive components like resistors, inductors & capacitors. To measure values of passive components, we use multimeter, bridges (for L&C) etc. In this unit, we will be studying Electronic Voltmeter (EVM), which is a more sensitive and hence accurate instrument as compared to Multimeter. EVM can also be used for very low current measurements by using a standard resistance. The power consumed by these circuits is of vital importance and hence we will also study the power meter. While studying the construction of power meter, we will see that the necessary torque required for meter movement is generated with the help of interaction of magnetic field and current and hence we will also discuss the art of measurement of magnetic field.

Objectives

After going through this unit, you will be able to understand

- basic construction, working and some of the applications of Oscilloscope,
- generation of various shapes of signals,

- accurate measurement of voltage using Electronic voltmeter,
- measurement of power, and
- measurement of magnetic field.

13.2 CATHODE RAY OSCILLOSCOPE

The cathode ray oscilloscope, generally referred to as the oscilloscope or simple "scope", is probably the most versatile electrical measuring instrument available. Some of the electrical parameters that can be observed with the oscilloscope are ac or dc voltage, indirect measurement of ac or dc current, time, phase relationships, frequency, and a wide range of waveform evaluations such as rise time, fall time, ringing, and overshoot. The oscilloscope consists of the following major subsystems:

- Cathode ray tube or CRT
- Vertical amplifier
- Horizontal amplifier
- Sweep generator
- Trigger circuit
- Associated power supplies

The heart of the instrument is the cathode ray tube. The remaining sub-systems are necessary for signal conditioning so that a visual representation of the input signal will be displayed on the face of the CRT.

13.2.1 Cathode Ray Tube (CRT)

The cathode ray tube used in an oscilloscope is very similar to the picture tube in a television set. A cross sectional representation of a CRT is shown in Fig.13.2. Major components of a general purpose CRT are:

- Evacuated glass envelope
- Electron gun assembly
- Deflection plate assembly
- Phosphor coated screen

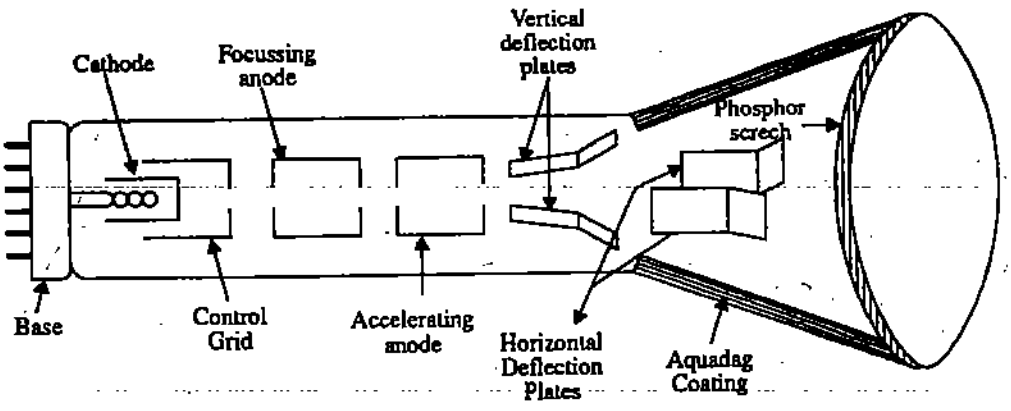


Fig.13.2 : Cathode ray tube with major components identified.

The glass envelope is evacuated to a fairly high vacuum to permit the electron beam to traverse the tube easily. Most laboratory quality oscilloscopes use a CRTwhich has circular screen approximately 5 inch in diameter. All electrical connections except the high-voltage connection are made through the base of the CRT.

The electron gun assembly consists of an indirectly heated cathode and the necessary heater, a control grid, focussing anode and accelerating anode. The purpose of the electron gun assembly is to provide a source of electrons, converged and focussed into a well-defined beam, which is accelerated towards the fluorescent screen. The electrons that make up the beam are given off by thermionic emission from the heated cathode. The cathode is surrounded by a cylindrical cap that is at a negative potential. This acts as a control grid. Because the control grid is at negative potential, electrons are repelled away from the cylinder walls and, therefore, stream through the hole where they move into the electric field of the focussing and accelerating anodes. The magnitude of the accelerating field is given by

$$E = \frac{V_a}{d}$$

where, V_a = accelerating anode voltage and d = distance between the cathode and second anode measured in meters. When electrons enter the electric field, which is assumed to be of uniform intensity, a force will be exerted on the electrons that will accelerate them along the axis of the tube. The magnitude of the force is given by

$$F = EQ = ma \Rightarrow a = \frac{EQ}{m}$$

where E = electric field intensity and Q = electronic charge = 1.6×10^{-19} C, m = mass of electrons, a = acceleration produced due to electric field. Using the expression for electric field in above equation, we obtain

$$a = \frac{V_a Q}{dm}$$

During the period of acceleration, the electrons are gaining kinetic energy as they gain velocities. If v is the velocity acquired then,

$$\frac{1}{2}mv^2 = V_a Q \Rightarrow v = \sqrt{\frac{2V_a Q}{m}}$$

After the electrons leave the electron gun assembly at a speed given by above mentioned equation, they enter and pass through a region controlled by the deflection plates. One pair of plates control the vertical motion of the beam while the other pair controls the longitudinal component of the electron velocity. The deflection plates are described by two geometric parameters of length (L) of the plates and the plate separation (d). The deflecting action of the plates is dependent on the intensity of the electric field (E_d) between the plates given by

$$E_d = \frac{V_d}{d}$$

where V_d = magnitude of the deflecting voltage. This field will exert a force = $E_d Q$ on the electrons, deviating the beam from a straight line trajectory.

$$F_d = E_d Q = \frac{V_d}{d} Q = ma_y$$

$$\Rightarrow \quad a_y = \frac{V_d Q}{md} = \text{Acceleration along } y-\text{axis}$$

It can be shown that the lateral distance travelled by electron is given by

$$h = \frac{V_d Q t^2}{2dm}$$

where t = time required for electrons to pass through the plates is given by

$$t = \frac{L}{v}$$

Here v is the velocity of electrons when it comes out of electron gun assembly.

Combining these equations, we get

$$h = \frac{L^2 V_d}{4 V_a d}$$

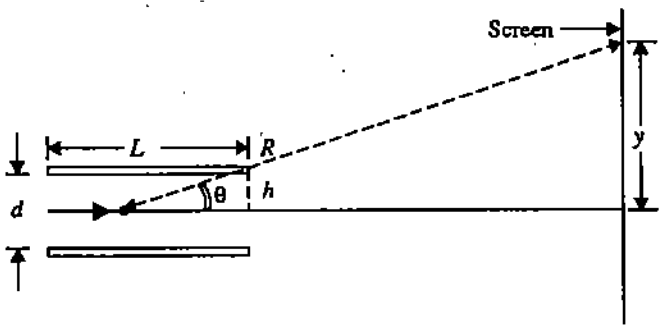


Fig.13.3 : Deflection of electron beam in CRT.

From Fig. 13.3

$$\theta = \frac{h}{L/2} = \frac{2h}{L} = \frac{y}{R}$$

$$\Rightarrow y = \frac{2hR}{L}$$

$$= \frac{RLV_d}{2V_a d}$$

$$\Rightarrow \frac{V_d}{y} = \frac{2V_a d}{RL}$$

The term $\frac{V_d}{y}$ is referred to as "deflection sensitivity" and is defined as voltage required per unit deflection. When the electron beam strikes the phosphor-coated face of the CRT, a spot of light is produced due to "fluorescence" as phosphor is a florescent material. The high velocity electrons that strike the phosphor coated face of the CRT are either repelled by the collision or cause secondary emission of electrons to maintain electrical equilibrium of the screen. To provide return path to ground for these electrons, the inside surface of the CRT is coated with graphite called "aquadag".

13.2.2 The Basic Oscilloscope

The CRT and the associated controls for accelerating, deflecting and focussing the electron beam, permit us to obtain a lighted spot on the screen. To be of practical use as a measuring instrument, we must connect additional electronic circuitary to the CRT to provide a means of very fast deflection and control of the electron beam. The purpose of the electronic circuits is to cause the beam to trace on the CRT screen a reproduction of the signal we apply to the input terminals of the oscilloscope. A block diagram of a basic oscilloscope is shown in Fig. 13.4(a).

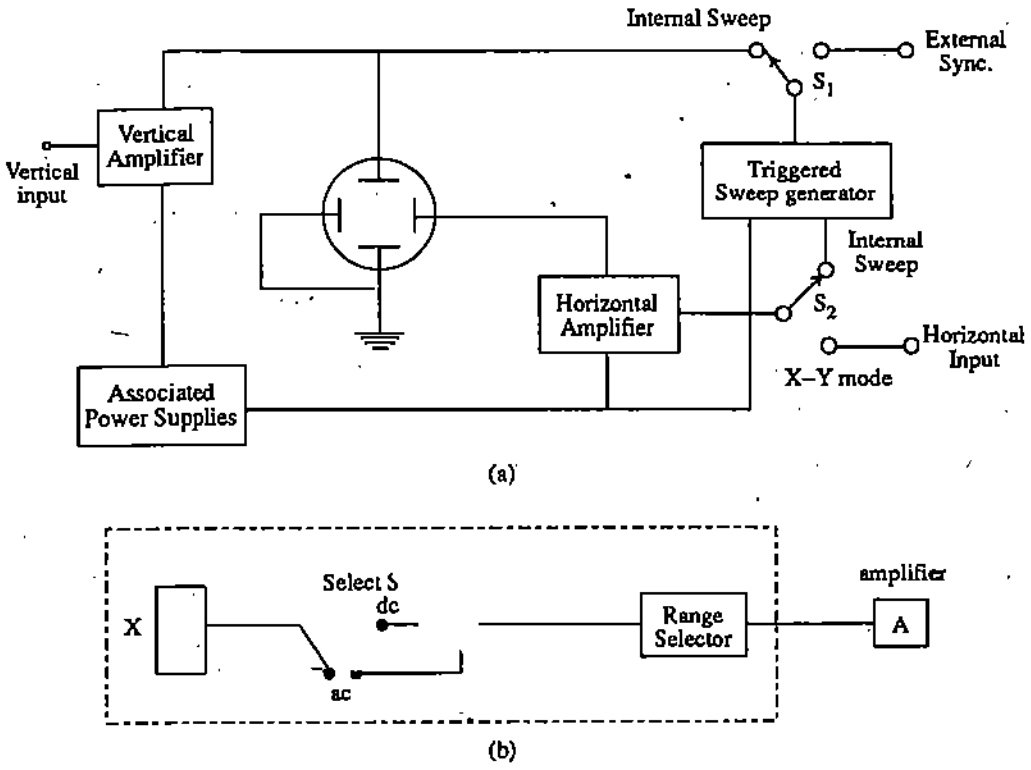


Fig.13.4 : (a) Block diagram of a basic cathode ray oscilloscope (b) Input to amplifier of vertical plate.

A signal to be displayed on the CRT screen is applied to the **vertical input terminal** where it is fed into the vertical amplifier. The signal is amplified and applied to the vertical deflection plates, which causes the beam to be deflected in the vertical plane.

Input to the Amplifier of Vertical Plate

The external signal is applied to the terminal marked x-input as shown in Fig. 13.4 (b). The select switch is put on the position ac or dc depending on the signal we are measuring. The input amplifier to the y-plate is normally calibrated for a standard input range of amplifier A. For higher voltage measurement we have a range selector which basically attenuates the signal to the desired input at A (we have already studied filters and attenuators).

Input to the Amplifier of Horizontal Plate

As can be seen in Fig. 13.4 (a), the output of the vertical amplifier is connected to the internal sync position of switch S_1. With the switch set to internal sync, as it is for normal operation of the oscilloscope, the output of the vertical amplifier is applied to the sweep generator. The input voltage waveform irrespective of shape at a particular value triggers the switch, which creates pulses and these pulses are then fed to the Sawtooth generator circuit and that provides the ramp signal. This signal triggers the sweep generator as shown in Fig. 13.5.

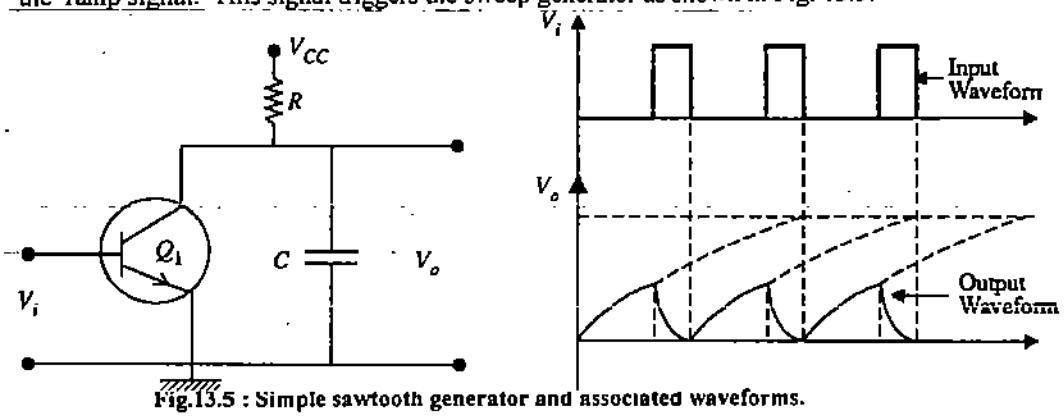


Fig.13.5 : Simple sawtooth generator and associated waveforms.

The purpose of sweep generator is to develop a voltage at the horizontal deflection plate that increases linearly with time. This linearly increasing voltage, called a 'ramp-stage' or a 'Sawtooth waveform', causes the beam to be deflected equal distances horizontally per unit time. The pulse for sawtooth generation can also be given by external source to which the input is synchronized (the sawtooth signal at the x-plate is generated at the same time the wave form at y-plate starts). Normally we use oscilloscope in internal synchronization mode. The horizontal amplifier serves to amplify the signal at its input prior to the signal being applied to the horizontal deflection plate.

The function of switch S_2, is to either generate sawtooth wave in x-plate, or put a direct signal to the x-plate of the oscilloscope. The sine wave from two oscillators can be introduced in x and y-plates of oscilloscope to get Lissajous figures, which allows measurement of frequency. The input signal to the horizontal amplifier depends on the position to which switch S_2 is set.

13.2.3 Laboratory Oscilloscopes

(i) Dual-trace Oscilloscope

A dual trace is obtained by electronically switching the single electron beam. Fig. 13.6 shows a block diagram of the two vertical input channels and the electronic switch that alternately connects the two input channels to the vertical amplifier. There are generally at least four modes of operation with dual-trace oscilloscopes; they are labeled A, B,

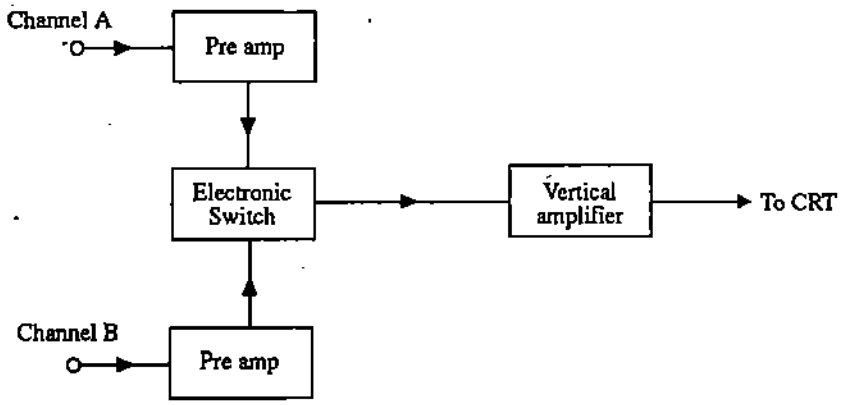


Fig.13.6 : Block diagram of the input channels of a dual trace oscilloscope.

alternate, and chopped. When set to A or B, only the input at that channel is displayed. In the alternate mode the inputs are displayed on alternate traces. Since the switching rate is synchronised with the sweep generator, switching occurs at the same rate as the output of the sweep generator. The "alternate mode" of operation is generally preferred when displaying relatively high-frequency signals. In the "chopped mode", electronic switching occurs at a rate completely independent of the sweep rate, and therefore each display has portions missing during which time the other signals is being displayed. The chopped mode is normally used at low sweep rates when the alternate mode would provide a display with appreciable flicker.

(ii) Storage Oscilloscope

There are many oscilloscope applications where the limited persistence of the CRT phosphor makes real time observation of one-time events nearly impossible. Although such events can be recorded photographically, this may prove to be fairly expensive and time consuming. The storage oscilloscope makes it possible to retain a CRT display for an extended period of time. The storage CRT uses two electron guns, the usual electron gun called a writing gun and a flood gun which uniformly bombards the entire CRT

screen with low-energy electrons. The phosphor partjcles struck by these low energy electrons takes on a fairly low-level charge; however, unenergised particles remains in a no-change condition. When a trace is to be recorded, the writing gun is turned on and high energy electrons strike the screen forming an image. The screen is erased by grounding the phosphor screen, which removes excess charge.

13.2.4 Measurement of Voltage, Current and Time

The range of applications of oscilloscopes varies from basic voltage, time, frequency measurements and wave form observations to highly specialised applications in all areas of science, engineering and technology.

Voltage measurements

The most direct voltage measurement made with an oscilloscope is the peak-to-peak value. The rms value of the voltage can easily be calculated from the peak-to-peak measurements if desired. To arrive at a voltage value from the CRT display, one must observe the setting of the vertical attenuator, expressed in volts/div, and the peak-to-peak deflection of the beam. The peak-to-peak value of the voltage is then computed as (see Fig. 13.7)

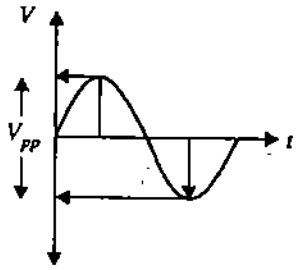


Fig. 13.7 : Voltage measurement.

$$V_{P\text{-}P} = \left(\frac{\text{volts}}{\text{div}}\right) \times \text{no.of div}$$

This can be easily explained with the example 13.1.

Example 13.1

Let the waveform shown in Fig. 13.8 is observed on the screen of an oscilloscope. If the vertical attenuator is set to 0.5 volts/div, find the peak to peak amaplitude of the signal.

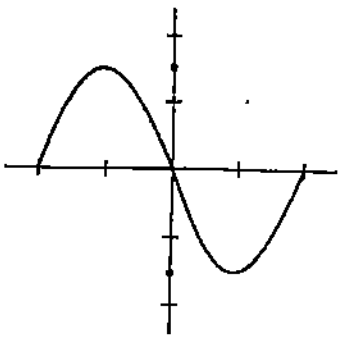


Fig.13.8

Solution :

$$V_{p-p} = \frac{\text{volts}}{\text{div}} \times \text{no.of div}$$

$$= \frac{0.5v}{\text{div}} \times 3\text{div}$$

$$= 1.5 \text{ V}$$

Period and Frequency Measurements

The period and frequency of periodic signals are easily measured with the oscilloscope. The waveform must be displayed in such a manner that one complete cycle is displayed on the CRT screen. Accuracy is generally improved if the single cycle displayed fills as much of the horizontal distance across the screen as possible. The period is calculated as follows:

$$T = \left(\frac{\text{time}}{\text{div}}\right)\left(\frac{\text{no.of div}}{\text{cycle}}\right)$$

The frequency is then computed as the reciprocal of the period.

$$f = \frac{1}{T}$$

13.2.5 Digital and Storage Oscilloscope

The storage oscilloscope described in earlier section are quite expensive and are now being replaced by digital oscilloscope. In these oscilloscope the signal on screen is sampled and digitized. The amplitude and time base per cm are displayed in numbers at a corner of the screen. The digitized signal can be put into a memory (like computer memory) and recalled (D/A converter) to display when desired. Thus they also serve as storage oscilloscope.

SAQ 1

Draw a pictorial representation of a general purpose CRT and label the components by name.

SAQ 2

Describe the basic principle of operation of dual-trace/storage oscilloscope.

SAQ 3

If the time/div control is set to 2μs/div and the displayed signal covers 4 div on the horizontal scale of the CRT screen, determine the frequency of the signal.

SAQ 4

Explain the principle of Digital Oscilloscope.

13.3 SIGNAL GENERATORS

A signal source is a vital component at a test set up. Signal sources provide a variety of waveforms for testing electronic circuits, usually at low power. A function generator is an instrument that provides variety of output waveforms over a wide range of frequency. The most common output waveforms are **Sine, pulse, triangular, ramp**. The frequency range generally extends from a fraction of a Hertz to atleast several hundred kilohertz. The different wave shapes are given in Fig. 13.9.

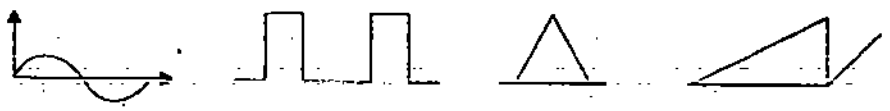


Fig. 13.9 : Different shapes of wave form. (a) Sinusoidal (b) Rectangular (c) Triangular (d) Ramp.

Definition of rise time (T_r): Time taken by the signal to rise from 10% to 90% of the maximum value of the signal is called rise time.

Fall time (T_f): Time taken by the signal to fall from 90% to 10% of the maximum value of the signal is called fall time.

There are several circuits to provide such waveforms individually. For example, you are aware that an LC oscillator can provide sine wave while multivibrator can provide pulses. However, by starting from any particular waveform we can with proper circuitary, generate other waveforms. In a function generator, a simple instrument is capable of providing different types of waveform. The most commonly used circuit is described below. .

Function generator:

The primary waveform in the circuit shown is a square wave. This is because some square wave generator circuits offer significantly better amplitude and frequency stability characteristics with simpler circuits than sine wave generating circuits.

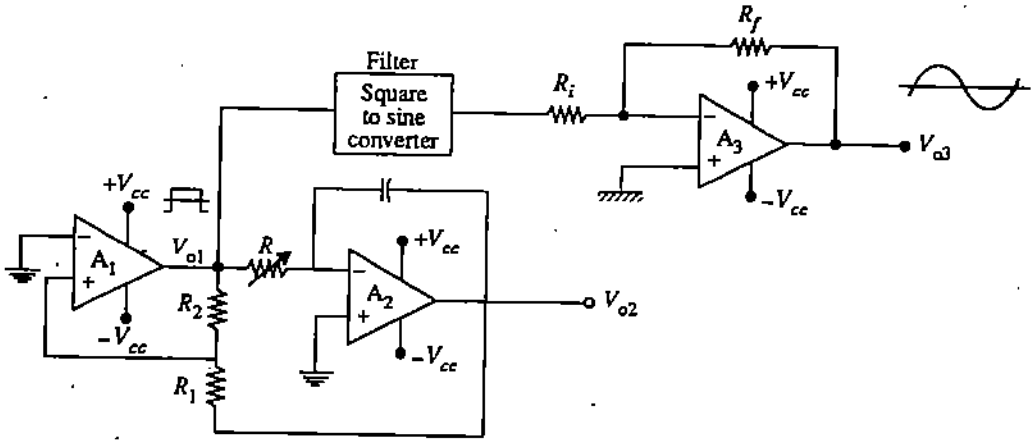


Fig.13.10 : Circuit of a basic function generator.

Working of the Circuit

The first stage A_1, which is a voltage comparator, generates a square wave output V_{01}. The output of A_1 is driven to saturation; therefore the square wave is either at $+V_{CC}$ or $-V_{CC}$ as shown in Fig. 13.11. The second stage, A_2, is an integrator that generates a triangular output at V_{02} as discussed later.

The square wave is also applied to a square-to-sine wave converter that filters out the odd harmonics making up the square-wave while passing only the fundamental sine wave. You will learn later that the square waves are produced by the combination of several sine waves, and by differentiation and integration we can convert pulses to triangular waves and vice-versa.

The operation of the circuit can be analysed by starting at the output of the comparator, which is either $+V_{CC}$ or $-V_{CC}$. Consider V_{01} to be at $-V_{CC}$. The voltage V_{01} will remain at $-V_{CC}$ until the voltage at the inverting input of A_1 exceeds the voltage at the non-inverting input, which in this case is at zero volts. The non-inverting input voltage, V_x, is due, in part, to the voltage V_{01} and, in part, to the voltage V_{02} and is given by

$$V_x = -V_{CC}\left(\frac{R_1}{R_1 + R_2}\right) + V_{02}\left(\frac{R_2}{R_1 + R_2}\right)$$

The output V_{01} changes state when $V_x = 0$, therefore

$$0 = -V_{CC}\left(\frac{R_1}{R_1 + R_2}\right) + V_{02}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$\Rightarrow V_{CC}R_1 = V_{02}R_2$$

$$\Rightarrow V_{02} = V_{CC}\left(\frac{R_1}{R_2}\right)$$

The above expression determines the maximum amplitude of the triangular output, V_{02}. When output V_{02} reaches peak value, the output of the comparator changes states and the triangular wave begins to decrease linearly. The waveforms at V_{01}, V_{02} and V_x are shown in Fig. 13.11 for the case where $R_1 = R_2$.

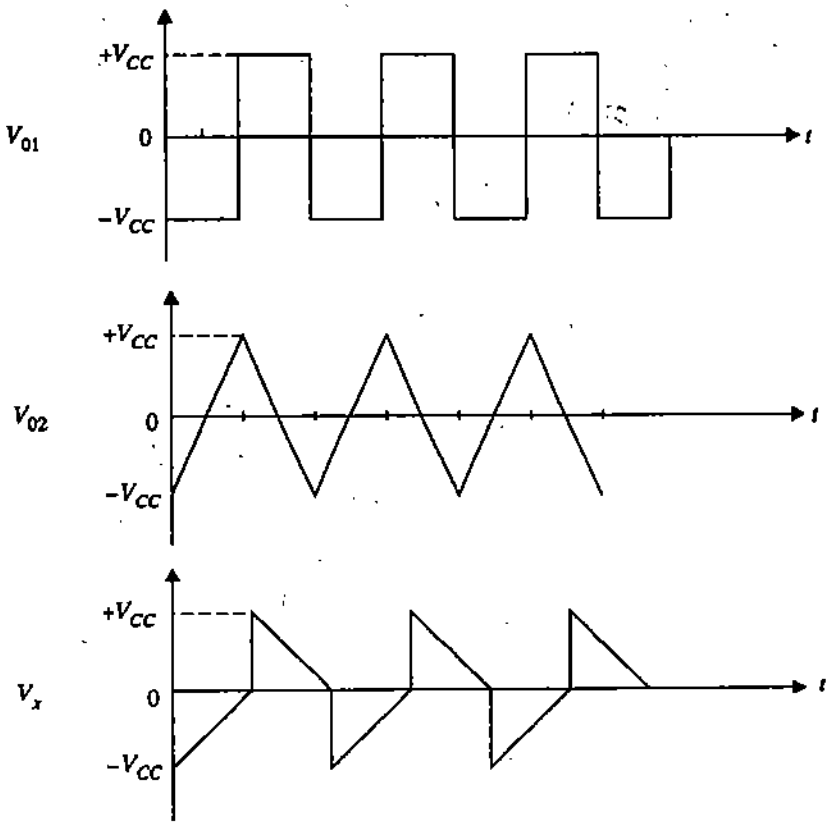


Fig.13.11 : Output waveforms for function generator.

The frequency of the circuit is controlled by the *RC* time constant of the integrator. To obtain an expression for the frequency, we begin with the expression relating capacitor current:

$$q = i_c t$$

$$\Rightarrow dq = i_c dt \Rightarrow i_c = \frac{dq}{dt}$$

Also, $$q = CV_{02}$$

$$\therefore i_c = \frac{d}{dt}(CV_{02}) = C\frac{dV_{02}}{dt}$$

Since the input resistance of the operational amplifier is very high, the current through resistor R is approximately equal to the charging current of the capacitor, therefore, we

can write

$$i_R \approx i_c = C\frac{dV_{02}}{dt}$$

Also, since the voltage gain of the operational amplifier is very high, the voltage at the input of the amplifier is very nearly zero, therefore,

$$i_R = \frac{V_{01} - 0}{R} = C\frac{dV_{02}}{dt}$$

$$\Rightarrow dV_{02} = \frac{1}{RC}V_{01}dt$$

Integrating both sides,

$$\int dV_{02} = \frac{1}{RC}\int V_{01}\,dt = \frac{V_{01}}{RC} \times t$$

$$\Rightarrow V_{02} = \frac{V_{01} \times t}{RC}$$

We know,

$$V_{02} = V_{CC}\left(\frac{R_1}{R_2}\right)$$

$$\therefore V_{CC}\left(\frac{R_1}{R_2}\right) = \frac{V_{01}t}{RC}$$

$$\Rightarrow t = RC\left(\frac{R_1}{R_2}\right) \text{ as } V_{01} = V_{CC}$$

The above equation has been deduced assuming no initial charge and therefore no initial voltage on the capacitor. Therefore, the time t given above is the time for the capacitor to change from 0V until switching occurs, which is 1/4 cycle. Since $t = T/4$,

$$\therefore \frac{T}{4} = RC\left(\frac{R_1}{R_2}\right) \Rightarrow T = 4RC\left(\frac{R_1}{R_2}\right)$$

$$\therefore f = \frac{1}{T} = \frac{1}{4RC}\left(\frac{R_2}{R_1}\right)$$

Pulse Generators

Pulse generators are instruments that produce a rectangular waveform similar to a square wave but of different duty cycle. Duty cycle is defined as the ratio of the pulse width to the pulse period, expressed in percent.

$$\text{Duty cycle} = \frac{\text{Pulse width}}{\text{Pulse period}} \times 100$$

The duty cycle of a square wave is 50% whereas the duty cycle of a pulse is generally from approximately 5 to 95%.

The output of a stable multivibrator is a square wave. The duty cycle of the square wave can be varied by changing values of R and C.

SAQ 5

Describe the function generator.

SAQ 6

What is difference between a square wave and a pulse.

SAQ 7

Compute the frequency and the peak amplitude of the triangular output of the circuit shown in Fig 13.12.

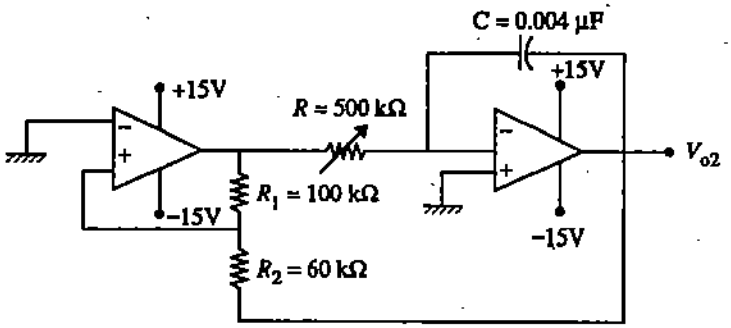


Fig. 13.12

13.4 ELECTRONIC VOLTMETER

Recall from class XII Physics course that the volt-ohm-milliammeter (VOM), is a rugged and accurate instrument, but suffers from certain disadvantages. The main problem is that it lacks both sensitivity and high input resistance. (A sensitivity of 20,000 Ω /V with a 0 to 0.5 V range has an input impedance of only 0.5×20,000 = 10 KΩ. The electronic voltmeter (EVM), on the other hand, can have an input resistance ranging from 10 to 100 MΩ, and input resistance will remain constant over all ranges instead of being different on each range as in the VOM. The EVM presents less loading to circuit under test than the VOM. The original EVMs used vacuum tubes, so they were called vacuum tube voltmeters (VTVM). With the introduction of the transistor and other semiconductor devices, vacuum tubes are no longer used in these instruments. We will discuss below in detail the differential amplifier type of EVM.

The Differential-Amplifier type of EVM

The field effect transistors (FET) can be used to increase the input resistance of a dc voltmeter. Fig. 13.13 shows the schematic of a difference amplifier using field-effect transistor.

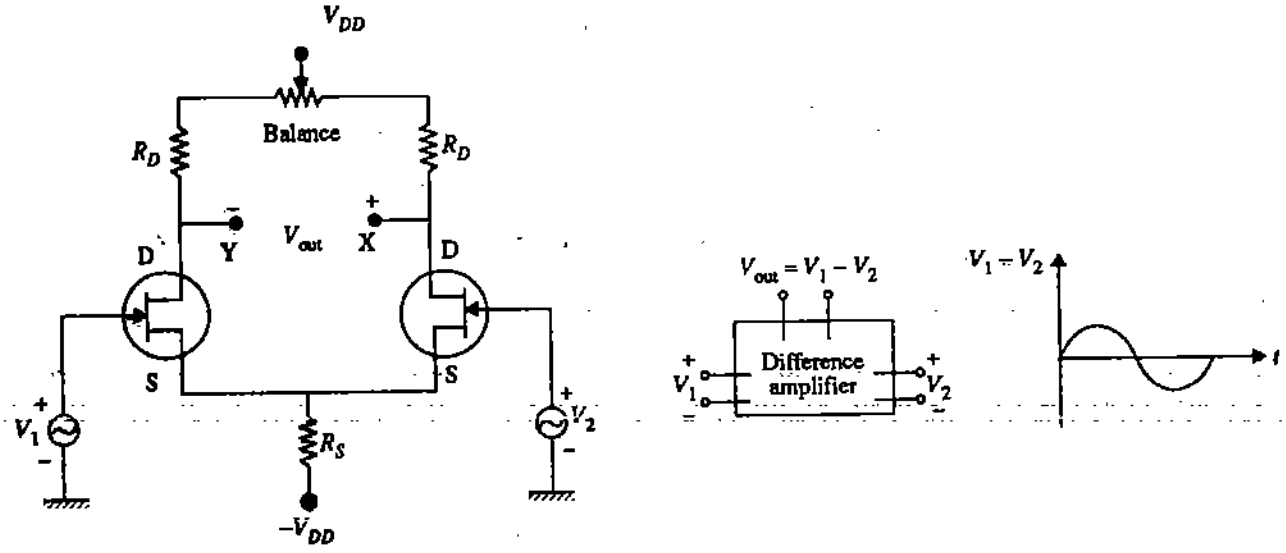


Fig.13.13 : Difference amplifier with balance adjustment.

This circuit also applies to a difference amplifier with bipolar junction transistors (BJTs). The circuit shown here consists of two FETs that should be reasonably matched for current gain to ensure thermal stability of the circuit. Therefore, an increase in source current in one FET is offset by a corresponding decrease in the source current of the other FET. The two FETs form the lower arms of the bridge circuit. Drain resistors R_D together form the upper arms. The meter movement is connected across the drain terminals of the FETs, representing two opposite corners of the bridge.

The circuit is balanced when identical FET's are used so that for a zero input there is no current through ammeter. If a positive dc voltage is applied to the gate of the left FET, a current will flow through the ammeter in the direction shown in Fig. 13.14.

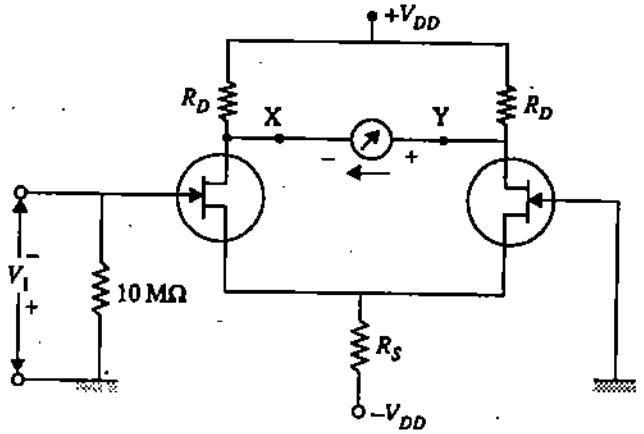


Fig.13.14 : The difference amplifier type EVM.

The size of the current depends on the magnitude of the input voltage. By properly designing the circuit, the ammeter current will be directly proportional to the dc voltage across the input. Thus, the ammeter can be calibrated in volts to indicate the input voltage.

By using Thevenin's theorem, we can find the relation between the ammeter current and the input dc voltage, where ammeter is considered as the load. To determine V_{Th}, we remove the ammeter and the output voltage is the voltage gain of a single FET times the difference of V_1 & V_2. Since V_2 is zero, the output voltage under open circuit condition is

$$V_{out} = g_m \left(\frac{r_d R_D}{r_d + R_D} \right) V_1 = g_m \left(r_d \,||\, R_D \right) V_1$$

where r_d is the ac drain resistance, g_m= transconductance. To find the Thevenin resistance at terminals XY, we first set V_1 and V_{DD} equal to zero. Under this condition, both the FETs have a resistance of r_d as shown in Fig. 13.15. Assuming R_S to be relatively large,

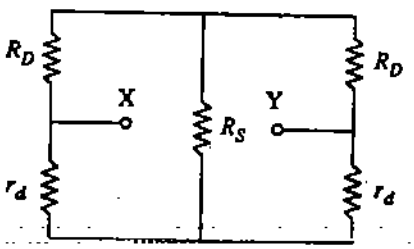


Fig.13.15 : Setting all voltages equal to zero to find R_{Th} of EVM.

$$R_{Th} = 2\,r_d \parallel 2\,R_D = 2\,(r_d \parallel R_D)$$

$$= 2\left(\frac{r_d\,R_D}{r_d + R_D}\right)$$

The Thevenin equivalent circuit with ammeter connected as a load is shown in Fig.13.16.

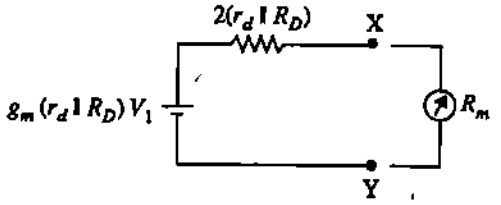


Fig.13.16 : Equivalent circuit of EVM.

From Fig. 13.16 the current through ammeter is found as:

$$i = \frac{V_{out}}{R_{Th} + R_m} = \frac{g_m\left(r_d \parallel R_D\right)}{2\left(r_d \parallel R_D\right) + R_m} V_1$$

where R_m = meter resistance.

If $R_D << r_d$, the above equation simplifies to

$$i = \frac{g_m R_D}{2R_D + R_m} V_1$$

This equation relates ammeter current to the input dc voltage.

SAQ 8

How does FET EVM differs from the VOM?

SAQ 9

Give circuit for the difference-amplifier type of EVM.

SAQ 10

Given a difference amplifier type of FET voltmeter, find the ammeter current under the following conditions:

$V_1 = 1\text{V}$ $\qquad R_D = 10\ \text{K}\Omega$

$r_d = 100\ \text{K}\Omega$ $\qquad R_m = 50\ \text{M}\Omega$

$g_m = 0.005$ Siemens

13.5 POWER METER

Wattmeter is an instrument to measure the power or rate of consumption of electricity in a circuit in watts. The most commonly used powermeter is Siemen's wattmeter shown in Fig. 13.17.

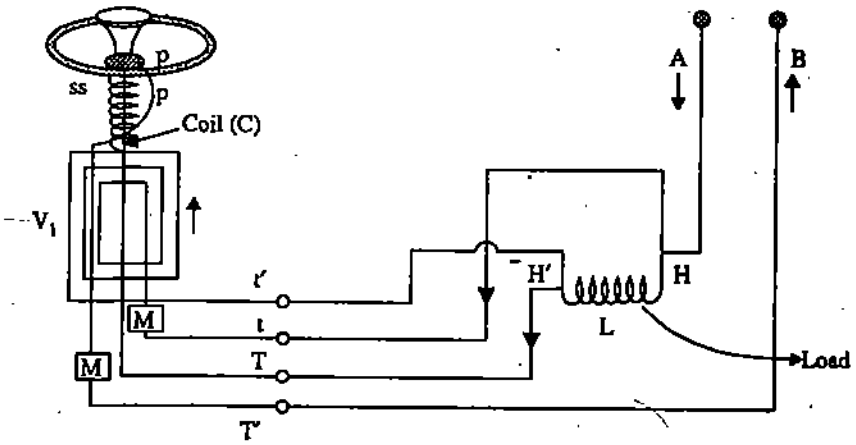


Fig.13.17 : Siemen's Wattmeter.

The Siemen's Wattmeter is identical in principle with Siemen's electrodynamometer. It consists of two coils at right angles to one another. One coil C is movable and the other, V is fixed. The moving coil C is of low resistance and is inserted in the main circuit. The high resistance fixed coil V, is joined as a shunt (i.e. in parallel) to that part of the circuit for which the power consumption is required. In Fig. 13.17, this part is an electric lamp (L). On closing the circuit, the main current i passes through the moving coil and a small current, proportional to the voltage E across the lamp terminals, passes through V. The turning moment is proportional to the product of these two i.e. proportional to Ei or the Watts used in L. When the moving coil is brought back to its normal position by turning the torsion head and its pointer through an angle say θ, the turning moment is balanced by the torsional moment. Since torsional moment is proportional to θ ,

$$Ei \propto \theta$$

or Watt expended in L = $K\theta$

Where the constant of proportionality K is a constant of the instrument and must be determined experimentally.

13.6 MAGNETIC FIELD METER

There are several techniques for the measurement of magnetic field. These are based on the change in the resistance of a material (magneto-resistance) under the application of magnetic field, or the voltage developed across a semiconductor under magnetic field (Hall effect). The instruments based on these principles will form a subject of study at higher level. In this section we shall discuss a method which is based on electromagnetic induction or the voltage developed across a coil when flux changes through a coil. The change of flux can be produced by moving the coil across a magnetic field. This method is often called determination of magnetic field by search coil.

A fluxmeter, an important instrument for measuring magnetic field strengths, has the same principle as that of a ballistic galvanometer. Fluxmeter consists of a moving coil suspended by a single silk fibre without torsion, the upper end of the fibre being connected to a fixed flat spring as shown in Fig. 13.18 (a) below.

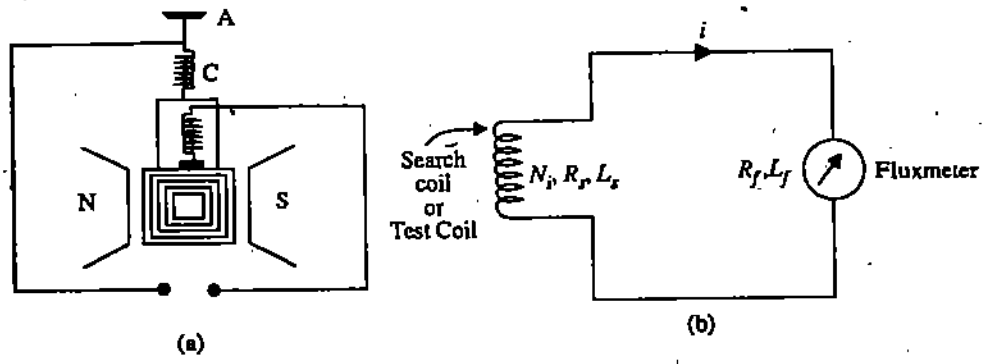


Fig.13.18 : (a) Construction of Fluxmeter (b) Fluxmeter in a circuit.

The coil is connected to the terminal X-X through two spirals C,C of thin silvered coil and is suspended in magnetic field of a permanent magnet NS. For direct measurement of the flux, a search coil is provided which can be connected to the terminals X,X as shown in Fig. 13.18 (b).

The expression for the change in magnetic flux of a fluxmeter can be derived as follows:

Let,

R_f = Resistance of fluxmeter

L_f = Self Inductance of fluxmeter

R_s = Resistance of search coil

N_1 = No. of turns in search coil

L_s = Self Inductance of search coil

The emf induced in the search coil is $-N_1 \frac{d\phi}{dt}$, where $\frac{d\phi}{dt}$ is the rate of change of flux in the search coil and the emf in fluxmeter coil is $G \frac{d\theta}{dt}$, where $\frac{d\theta}{dt}$ is angular velocity of the fluxmeter coil and $G = NAB$ is a constant depending on the construction of the fluxmeter. In addition, the emf produced in the circuit due to self inductances is $(L_f + L_s)\frac{di}{dt}$ or $L \frac{di}{dt}$, where L is the total inductance of the circuit. The potential drop in the resistance is $(R_f + R_s)\ i$ or Ri where R being total resistance of the circuit. Using Kirchoff's law, we get

$$-N_1 \frac{d\phi}{dt} + G\frac{d\theta}{dt} + L\frac{di}{dt} + Ri = 0$$

$$\Rightarrow N_1 \frac{d\phi}{dt} = G\frac{d\theta}{dt} + L\frac{di}{dt} + Ri$$

In practical applications, the potential drop in resistances $(=Ri)$ is small and can be neglected in comparisons to other terms, giving

$$N_1 \frac{d\phi}{dt} = G\frac{d\theta}{dt} + L\frac{di}{dt}$$

Integrating over time t, during which the flux change occurs,

$$N_1 \int_0^t \frac{d\phi}{dt} dt = G \int_0^t \frac{d\theta}{dt} dt + L \int_0^t \frac{di}{dt} dt$$

$$\Rightarrow N_1 \int_{\phi_1}^{\phi_2} d\phi = G \int_{\theta_1}^{\theta_2} d\theta + L \int_{i_1}^{i_2} di$$

$$\Rightarrow N_1 (\phi_2 - \phi_1) = G(\theta_2 - \theta_1) + L(i_2 - i_1)$$

Now, if we assume that the period in which the flux is changing is completely contained within the period (0-t) over which integration is carried, both the initial and final currents are zero, giving

$$N_1 (\phi_2 - \phi_1) = G (\theta_2 - \theta_1)$$

$$N_1 \Delta\phi = G\Delta\theta \Rightarrow \Delta\theta = \left(\frac{N_1}{G}\right)\Delta\phi$$

$$\Rightarrow \Delta\theta \propto \Delta\phi$$

which suggests that the deflection in the fluxmeter accurately follows any change in flux in the search coil.

13.7 SUMMARY

- Cathode ray oscilloscope is used for the measurement of electrical parameters like, ac and dc voltage, ac and dc current, time-phase relationship, frequency and for observing various wave forms.
- Laboratory oscilloscope can be classified into two categories: (i) Dual-trace oscilloscope (ii) Storage oscilloscope.
- Signal generator provides variety of output waveforms over a wide range of frequency. The most common output waveforms are: sine, pulse, square, triangular and ramp.
- Electronic voltmeter is characterised by high input resistance.
- Power meter is used to measure the power or rate of consumption of electricity in a circuit.
- Magnetic field meter is an instrument for measuring magnetic field strengths.

13.8 TERMINAL QUESTIONS

1) Explain the functioning of a general purpose CRO giving block diagram.

2) Explain the basic principle involved in dual trace CRO.

3) How a storage CRO works? Explain.

4) Describe in detail the functions of a function generator.

5) Describe in detail the functioning of Differential-amplifier type electronic voltmeter.

6) How a Siemens power meter works? Explain.

7) Give in detail how magnetic field can be measured with the help of a fluxmeter.

13.9 SOLUTIONS AND ANSWERS

SAQs

1. See text
2. See text
3.

$$T = \frac{2\mu\text{sec}}{\text{div}} \times \frac{4\text{div}}{\text{cyc}} = \frac{8\mu\text{sec}}{\text{cyc}}$$

$$\therefore \quad f = \frac{1}{T} = \frac{1}{8\mu\text{sec/cyc}} = 125\text{KHz}$$

4. See text
5. See text
6. See text
7. We know,

$$f = \frac{1}{4RC}\frac{R_2}{R_1}$$

$$= \frac{1}{4\times500\times10^3\times.004\times10^{-16}}\ \frac{100\times10^3}{60\times10^3}$$

$$= 208\text{Hz}$$

Also, $V_{02} = V_{CC}\left(\frac{R_1}{R_2}\right)$

$$= 15\left(\frac{60\times10^3}{100\times10^3}\right) = 9\text{V}$$

8. See text
9. See text
10.

$$i = \frac{g_m\left(r_d \| R_D\right)}{2\left(r_d \| R_D\right)+R_m}$$

Substituting all the values, we get

$$i = 2.5\text{ mA}$$

TQs

1. See text
2. See text
3. See text
4. See text
5. See text
6. See text
7. See text